harman kardon

Model DVD 47

DVD/CD/CD-R/CD-RW/VCD MP3 Player

Service Manual

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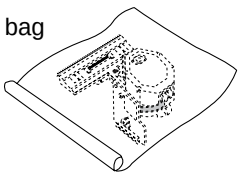
Rev0 7/2006

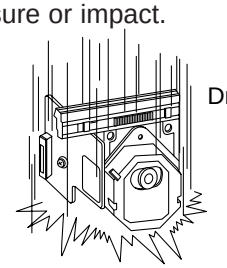
NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.

Storage in conductive bag

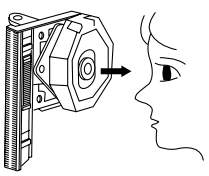




Drop impact

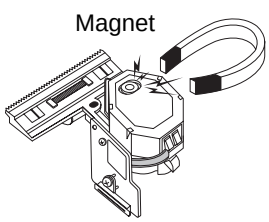
2. Repair notes

1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation
screws should absolutely never be touched.
4) Laser beams may damage the eyes!
Absolutely never permit laser beams to enter the eyes!
Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.

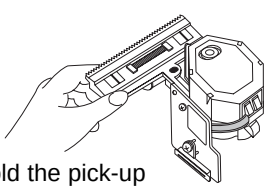


NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

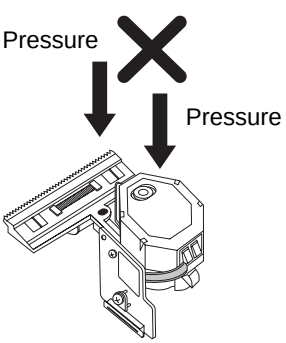
5) Cleaning the lens surface
If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.



Magnet

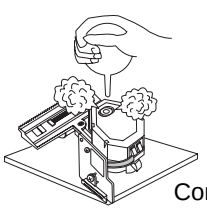


How to hold the pick-up

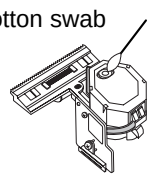


Pressure

Pressure



Conductive Sheet



Cotton swab

6) Never attempt to disassemble the pick-up.
Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

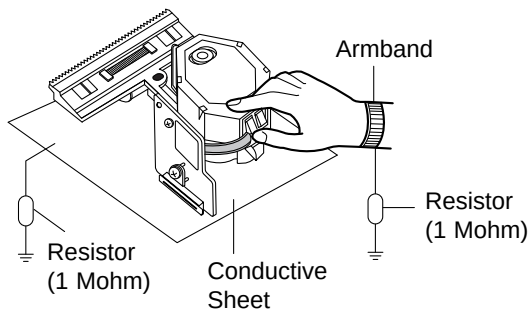
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1MΩ)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

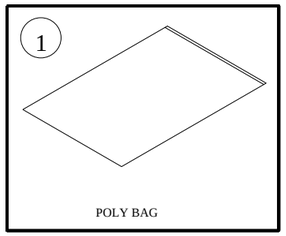
DVD 47 TECHNICAL SPECIFICATIONS

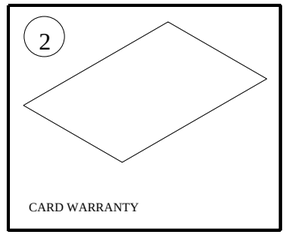
Applicable Disc:	Disc formats: 5-inch (12cm) or 3-inch (8cm) DVD-Video, DVD-Audio, standard-conforming DVD-R, DVD+R, DVD-RW, DVD+RW, SACD™, VCD, CD, CD-R, CD-RW or MP3 discs Region code: DVD Video disc with Code 1 or 0 only DVD-Layers: Single side/single layer, single side/dual layer, dual side/dual layer Audio formats: DVD-Audio MLP lossless, SACD 2-channel or multichannel, Linear PCM, MPEG, Windows Media® 9, Dolby Digital or DTS Audio discs Still-image format: JPEG
Video Signal System:	NTSC
HDMI™ Output:	Video: 480p, 720p, 1080i HDMI Version 1.0-compliant HDCP Version 1.1-compliant
Composite Video Output:	1V p-p/75 ohms, sync negative polarity
S-Video Output:	Y/Luminance: 1V p-p/75 ohms, sync negative polarity C/Chrominance: 0.286V p-p
Component Video Output:	Y: 1V p-p/75 ohms, sync negative polarity Pr: 0.7V p-p/75 ohms Pb: 0.7V p-p/75 ohms
Analog Audio Output:	2V rms (1kHz, 0dB)
Frequency Response:	DVD (Linear PCM): 2Hz – 22kHz +0/–0.5dB (48kHz sampling) 2Hz – 44kHz +0/–1.5dB (96kHz sampling) 2Hz – 88kHz +0/–0.5dB (192kHz sampling) CD: 2Hz – 20kHz +0/–0.5dB SACD: 2Hz – 100kHz +0/–0.5dB
Signal/Noise Ratio (SNR):	105dB (A-weighted)
Dynamic Range:	DVD: 100dB (18-bit)/105dB (20-bit) CD/DVD: 96dB (16-bit)
THD/1kHz:	DVD/CD: 0.0025%
Wow & Flutter:	Below Measurable Limits
AC Power:	110–240VAC/50–60Hz
Power Consumption:	1 Watt (On/Standby)/13 Watts (Max)
Dimensions (H x W x D):	2" x 17-3/10" x 11-1/4" (50mm x 440mm x 285mm)
Weight:	6 lb (2.7kg)
Shipping Dimensions (H x W x D):	5" x 14-3/8" x 20" (127mm x 365mmx 508mm)
Shipping Weight:	8.8 lb (4kg)

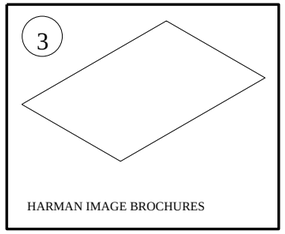
Depth measurement includes knobs and connectors.

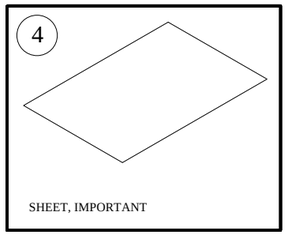
Height measurement includes feet and chassis.

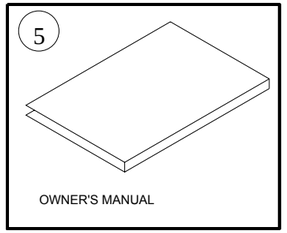
All specifications subject to change without notice.

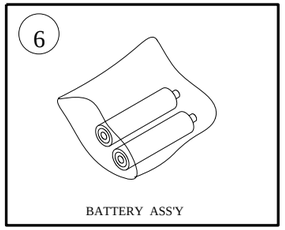


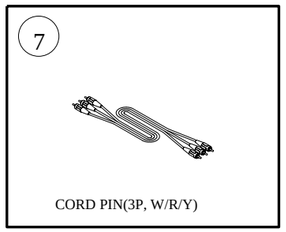


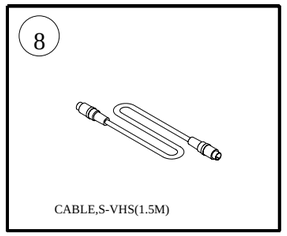


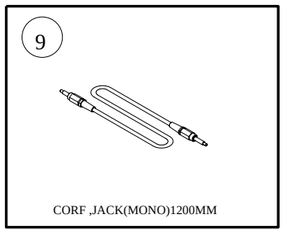


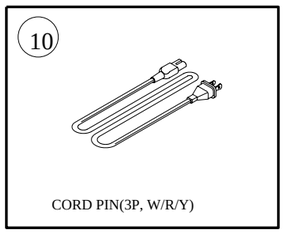


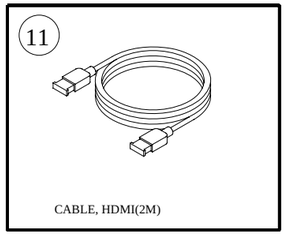


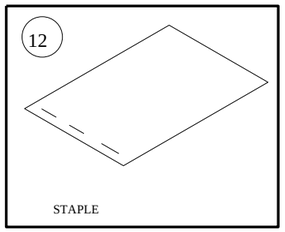






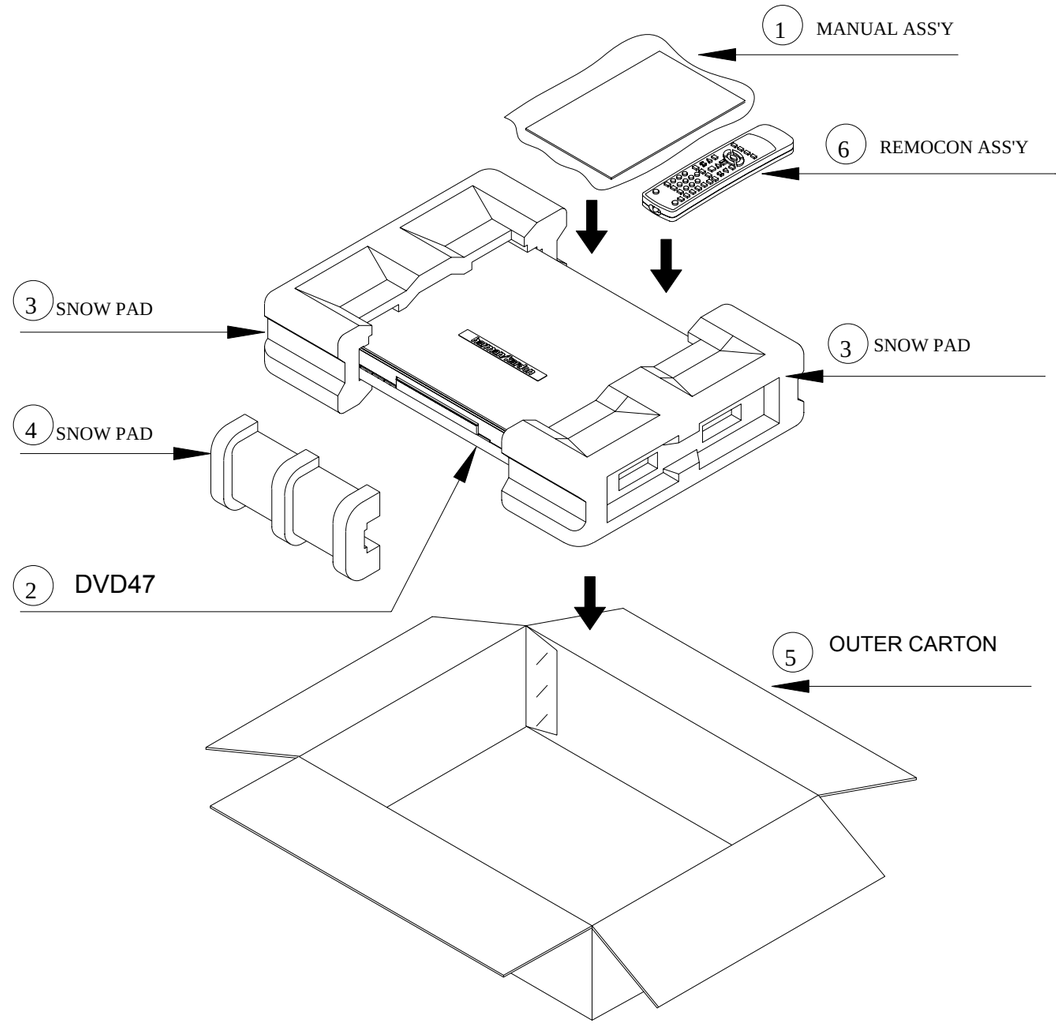






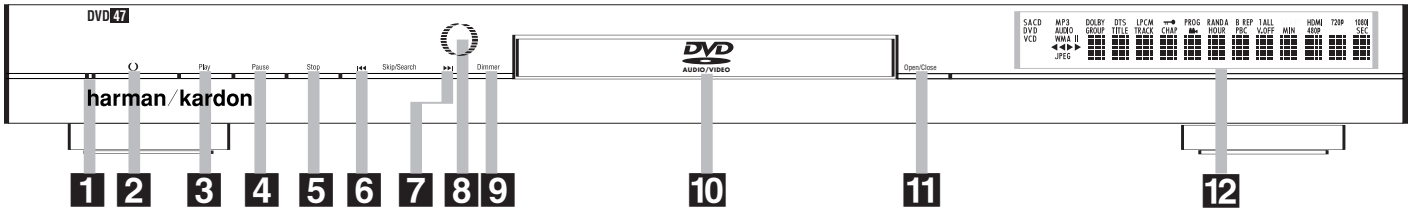
NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG		1
2	CARD WARRANTY	CQE1A172X	1
3	HARMAN IMAGE BROCHURES	HQE1A273Z	1
4	SHEET, IMPORTANT	CQE1A169Z	1
5	OWNER'S MANUAL	CQX1A1050Z	1
6	BATTERY		2
7	CORD,PIN(3P,W/R/Y)	CJS4S004Z	1
8	CABLE,S-VHS(1.5M)	CJS0I006Z	1
9	CORD,JACK(MONO)1200MM	CJS9D002Z	1
10	AC CORD	CJA2A085Z	1
11	CABLE,HDMI(2M)	CJS8T001Z	1
12	STAPLE		3

DVD 47 PACKAGING & ACCESSORIES



NO	DESCRIPTION	PARTS NO.	Q,ty
1	MANUAL ASS'Y		1
2	DVD47	DVD 47	1
3	SNOW,PAD	CPS1A714	2
4	SNOW,PAD	CPS1A715	1
5	DVD 47 OUTER CARTON	CPG1A798X	1
6	REMOCON ASS'Y	CARTDVD47	1
7			

FRONT-PANEL CONTROLS



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

1 Power Indicator
2 Power On/Off (Standby)
3 Play
4 Pause
5 Stop
6 Skip/Search Reverse
7 Skip/Search Forward
8 Remote Sensor
9 Display Dimmer
10 Disc Drawer
11 Open/Close
12 Information Display

1 Power Indicator: This indicator lights amber when the unit is connected to an AC power source, but is not turned on. When the unit is on, the indicator lights blue.

2 Power On/Off (Standby): Press the button once to turn the DVD 47 on. Press it again to put the unit in the Standby mode.

3 Play: Press to initiate playback or to resume playback after the **Pause Button 4 21** has been pressed.

4 Pause: Press this button to momentarily pause playback. To resume playback, press the button again. If a DVD is playing, action will freeze and a still picture will be displayed when the button is pressed.

5 Stop: Press this button once to place the disc in the Resume mode, which means that playback will stop, but as long as the tray is not opened or the disc changed, playback will continue from the same point on the disc when the **Play Button 3 23** is pressed again. Resume will also work if the unit was turned off. Resume will not operate for WMA files or VCDs that do not have playback control. To stop a disc and have play start from the beginning, press the button twice.

6 Skip/Search Reverse: Press this button once to return to the start of the current chapter for a DVD or track for a CD. Subsequent individual presses will skip backwards through the available chapters or tracks. Press and hold the button to play the disc in the fast reverse mode at the speed indicated in the on-screen display and by the **Playback Mode Indicators O**.

7 Skip/Search Forward: Press this button once to move to the start of the next chapter for a DVD or track for a CD. Subsequent presses will skip forward through the available chapters or tracks. Press and hold the button to play the disc in the Fast Play mode at the speed indicated in the on-screen display and by the **Playback Mode Indicators O**.

8 Remote Sensor: The sensor that receives commands from the remote control is behind the front panel in this area. To ensure proper operation of the player with the remote, it is important that this area not be covered. In the event that the player is enclosed in a cabinet or if the remote sensor is covered, you may extend the remote sensor by connecting an optional, external remote sensor to the **Remote Control Input 2** on the rear panel (see page 14). When optional, external IR "blasters" are used for system control, they should be positioned so that they point at this area.

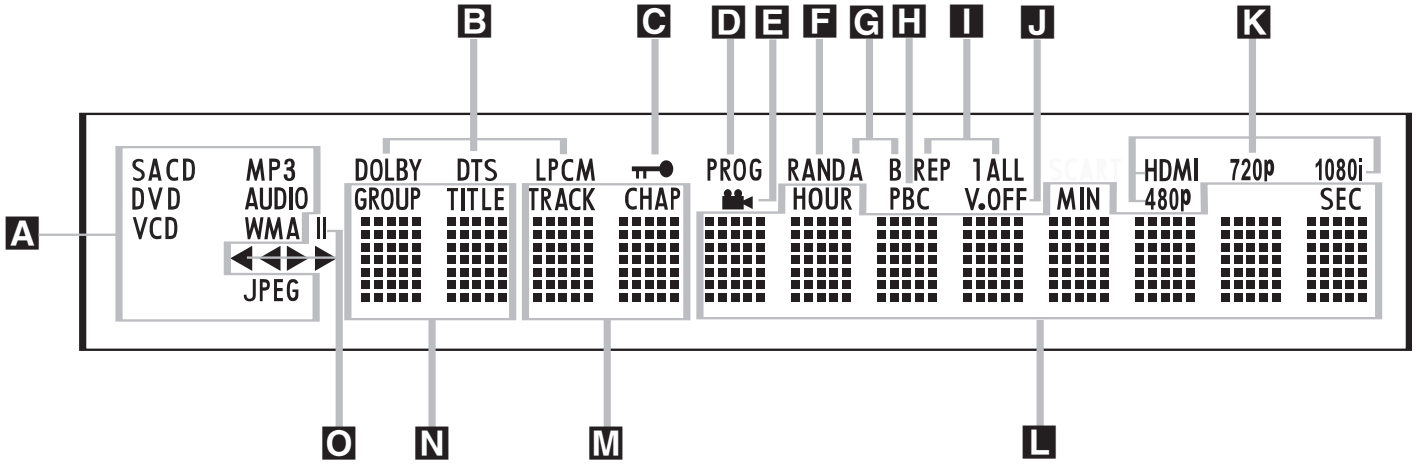
9 Display Dimmer: Press this button to reduce the brightness of the **Information Display 12** by 50% or to turn the display off completely in the following order: FULL BRIGHTNESS ➔ HALF BRIGHTNESS ➔ OFF ➔ FULL BRIGHTNESS.

10 Disc Drawer: This drawer is used to hold the discs played in the unit. Be certain to seat all discs carefully within the recess in the drawer. Do not press down on the drawer when it is open, to avoid damage to the player. When the drawer is left open with no activity for 5 minutes, it will automatically close to prevent dust or dirt from entering the component, and to prevent accidental damage. If a disc is present, the DVD 47 will immediately begin playback.

11 Open/Close: Press this button to open or close the disc tray.

12 Information Display: The Information Display provides status information on the player and the disc being played through a series of specific indicators and messages that appear in the display. See page 10 for more information on the display.

FRONT-PANEL INFORMATION DISPLAY



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A Disc-Type Indicators
B Audio Bitstream Indicators
C Parental Lock Indicator
D Program Indicator
E Angle Indicator
F Random Indicator
G A-B Repeat Indicator
H VCD Playback Control Indicator
I Repeat Indicators
J V-OFF Indicator
K Video Indicators
L Time Indicators
M Chapter/Track Number Indicators
N Group/Title Indicators
O Playback-Mode Indicator

A Disc Type Indicators: The **DVD**, **DVD-Audio**, **SACD**, **CD**, **VCD**, **MP3**, **WMA** or **JPEG** indicator will light to show the type of disc currently being played.

NOTE: The DVD 47 does not have an HDCD® (High Definition Compact Digital®) decoder. Therefore, to benefit from HDCD encoding, make sure to connect one of the DVD 47's **Digital Audio Outputs** ❹❺ to your receiver or processor with HDCD encoding. If your receiver or processor does not have HDCD decoding, you may still enjoy conventional CD playback of the disc.

B Audio Bitstream Indicators: When a Dolby® Digital, DTS® or linear PCM digital audio signal is present on the disc, one of these indicators will light. DVD-Audio, MP3 and WMA bitstreams will be indicated by the **Disc Type Indicator** **A**.

C Parental Lock Indicator: This indicator lights in red when the parental-lock system is engaged in order to prevent anyone from changing the rating level without a code.

D Program Indicator: This indicator lights when a playlist has been programmed using the menu system (available for CDs only). See page 36 for more information on programming playlists.

E Angle Indicator: This indicator blinks when alternative viewing angles are available on the DVD currently playing.

F Random Indicator: This indicator lights when the unit is in the Random Play mode.

G A-B Repeat Indicator: This indicator lights when a specific passage for repeat playback has been selected.

H VCD Playback Control Indicator: This indicator lights when the playback control function is turned on for VCDs.

I Repeat Indicators: These indicators light when any of the Repeat functions are in use.

J V-OFF Indicator: This indicator lights in red when the unit's video output has been turned off by pressing the **V-OFF Button** ⓰ on the remote control.

K Video Output Indicators: When the DVD 47 is connected to a video display using the **HDMI Output** ❸, the display sends information to the DVD 47 indicating the highest video resolution it is capable of handling, and the DVD 47 automatically sets the video output to match it. That resolution is displayed here. You may use the **HD Mode Selector** ⓱ to manually select a lower video output resolution.

L Time Indicators: These positions in the display will show the running time of a disc in play.

NOTE: The indicators **L M N** will also display text messages about the DVD's status, including `LOADING` when a disc is loading, `POWER OFF` when the unit is turned off, and `DISC ERROR` when a disc not compatible with the DVD is put into the play position.

M Chapter/Track Number Indicators: When a DVD disc is playing, these two positions in the display will show the current chapter. When a DVD-Audio, SACD or CD disc is playing they will show the current track number.

N Group/Title Indicators: These two positions in the display will show the current title number when a DVD disc is playing, or the current group for a DVD-Audio disc.

O Playback-Mode Indicators: These indicators light to show the current playback mode:

▶ Lights when a disc is playing in the normal mode. This indicator will flash when the disc is in Forward Slow Play mode. The on-screen banner display indicates the selected speed (1/2, 1/4, 1/8 or 1/16).

▶▶ When the DVD 47 is in the Fast Search play mode, two of these indicators will light to show that the unit is in a Fast Play mode. The on-screen banner display indicates the selected speed (x2, x4, x8, x20 or x100). Fast Play mode is not available for WMA files.

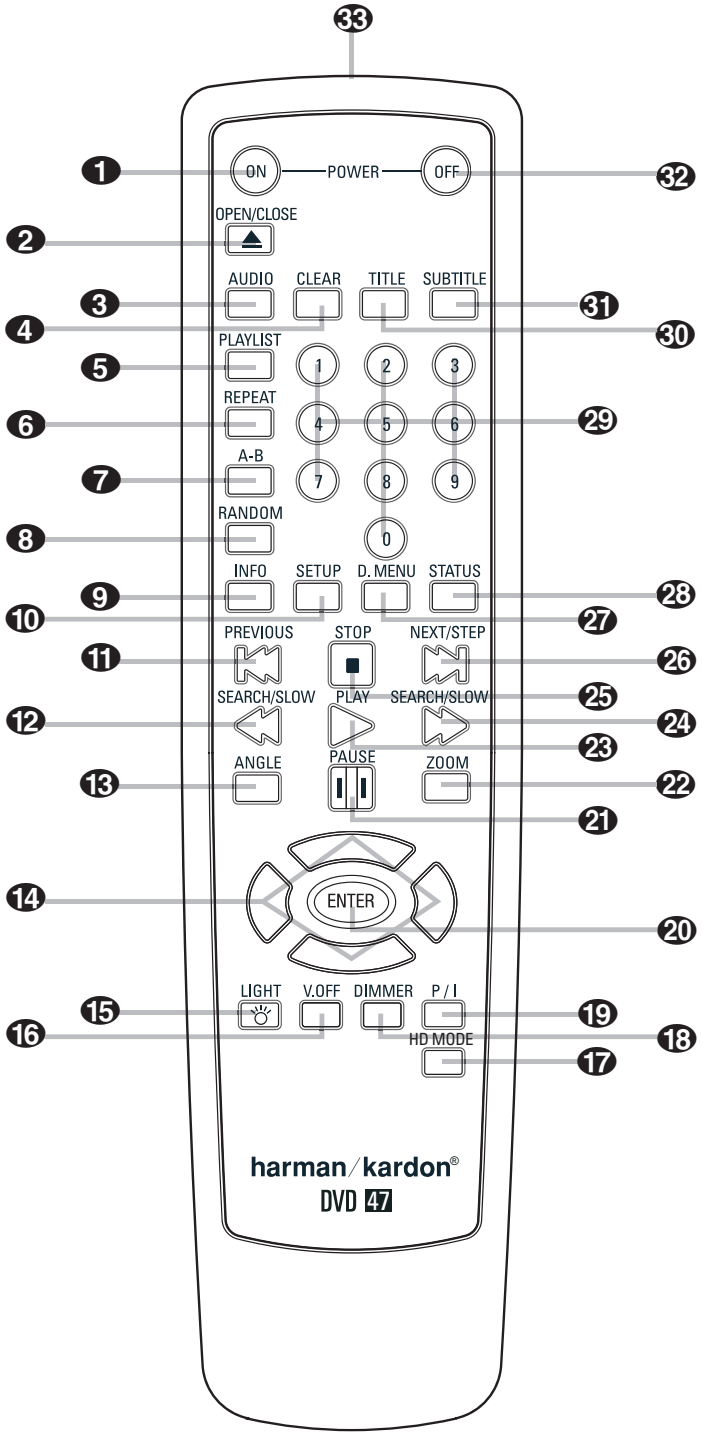
❙❙ Lights when the disc is paused.

◀◀ Lights when the disc is in the Fast Search Reverse mode. The on-screen banner display indicates the selected speed (x2, x4, x8, x20 or x100). Fast Search Reverse mode is not available for WMA files.

◀ Flashes when the disc is in Reverse Slow Play mode. The on-screen banner display indicates the selected speed (1/2 or 1/4).

REMOTE CONTROL FUNCTIONS

1. Power On
2. Open/Close
3. Audio Select
4. Clear
5. Playlist
6. Repeat
7. A-B Repeat
8. Random
9. Info
10. Setup
11. Previous Step/Skip
12. Search/Slow Reverse
13. Angle
14. ▲/▼/◀/▶ Navigation Buttons
15. Light
16. Video Off
17. HD Mode Selector
18. Dimmer
19. Progressive Scan/Interlaced
20. Enter
21. Pause
22. Zoom
23. Play
24. Search/Slow Forward
25. Stop
26. Next Step/Skip
27. Disc Menu
28. Status
29. Numeric Keys
30. Title
31. Subtitle
32. Power Off
33. IR Emitter



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REMOTE CONTROL FUNCTIONS

❶ **Power On:** Turns on the player when it is in Standby mode (Harman Kardon logo appears on-screen).

❷ **Open/Close:** Press to open or close the disc tray.

❸ **Audio Select:** Press to access various audio languages on a DVD (if the DVD contains multiple audio streams). This button may also allow you to access other audio formats on DVD discs, such as linear PCM or Dolby Digital 5.1 tracks (or other formats), if they've been recorded on the disc.

❹ **Clear:** Press this button to remove on-screen menus or banners from the display screen. Press this button to clear the current play order displayed next to a track while programming a playlist. In Stop mode and with all menus and banners removed from the display, press and hold this button for five seconds to reset all settings to their factory defaults.

❺ **Playlist:** Press this button to access the Playlist on-screen menu, which enables you to change the order in which tracks are played on a CD or DVD-Audio disc. (See page 36 for more information on creating and playing playlists.)

❻ **Repeat:** Each press of this button changes the playback mode to repeat a chapter or track or the entire disc. A repeat icon will appear in the upper right corner of the screen indicating the current repeat mode. If the Player Information Screen is active, the changes will be displayed on screen.

❼ **A-B Repeat:** Press this button to enter the starting point of a section on a disc you wish to repeat. The second press enters the end of the selection to be repeated. Once the "A" (start) and "B" (end) points have been entered the player will repeat the selection until the **Play Button** ㉓ 3 is pressed or the disc is stopped. If the Player Information Screen is active, the changes will be displayed on screen.

❽ **Random:** Each press of this button starts or stops playback in random order. The Random function is only available when playing CDs, but not when a Playlist is active (the Player Information screen indicates Programmed Order on the Playlist line).

❾ **Info:** Press once to access the Player Information menu for information on the current disc and the playback mode settings. Press again to remove information from screen. See page 28 for more information on the Player Information menu.

❿ **Setup:** Press this button to use the DVD 47's on-screen menu system to adjust the player's configuration settings. Note that the **Info Button** ❾ must be pressed to access the DVD 47's Player Information menu to obtain detailed disc information, and to configure the playback mode of the disc.

⓫ **Previous Step/Skip:** Press this button once to skip back to the beginning of the current chapter on a DVD or track on a CD or DVD-Audio disc. Press it again to continue to skip back through the previous chapters or tracks. After first pressing the **Pause Button** ㉑, press this button to step backwards through a DVD or VCD as a series of still image frames.

⓬ **Search/Slow Reverse:** This button initiates fast or slow play in the reverse mode. For fast reverse play, each press of the button when playing DVD or VCD discs changes the speed as indicated by the number appearing in the upper right corner of the screen. For slow reverse play, first press the **Pause Button** ㉑ and each subsequent press of this button will change the slow play speed as indicated by the number appearing in the upper right corner of the screen.

⓭ **Angle:** Press this button to change the camera angle on discs programmed for multiple-angle views. When a JPEG is being displayed, pressing the **Angle Button** ⓭ repeatedly causes the on-screen image to rotate clockwise by 90 degrees each press. The current orientation in degrees will be displayed in the upper right corner of the screen.

⓮ ◀▶▲▼ **Navigation Buttons:** Use to move the cursor in the on-screen menu system.

⓯ **Light:** Press to illuminate the buttons on the remote controller.

⓰ **Video Off:** Press this button to turn off the video output for improved audio performance when playing discs. Press it again to view the on-screen menus. It is highly recommended that you use this function to prevent "burn-in" of your plasma video display.

⓱ **HD Mode Selector:** When the DVD 47 is connected to a video display using the **HDMI Output** ❸, the display sends information to the DVD 47 indicating the highest video resolution it is capable of handling, and the DVD 47 automatically sets the video output to match it. Pressing this button allows you to manually change the output resolution, with your selection indicated by the **Video Output Indicators** K. The DVD 47 will not allow you to select a resolution beyond the capabilities of your display, and if you try to do so, an on-screen error message will appear to alert you to the selection of an incompatible video format. Changes made with this button remain active until the DVD 47 or the display is turned off. When either is turned off, and then on again, the DVD 47 will revert to the default setting transmitted by the display.

⓲ **Dimmer:** Press to change the brightness of the front panel display or to turn the display off completely in the following order: FULL BRIGHTNESS ➜ HALF BRIGHTNESS ➜ OFF ➜ FULL BRIGHTNESS

⓳ **Progressive Scan/Interlaced Button:** Each press of this button selects between the progressive scan and interlaced modes for the **Component Video Outputs** ❺. This button will not have any effect while the Setup menu system is active, indicated by -SETUP- appearing in the **Information Display** 12. Press the **Setup Button** ⓾ to clear the Setup menu, and then press this button to toggle between the progressive scan and interlaced component video settings.

⓴ **Enter:** Press this button to enter a setting in the DVD 47 menu system or to confirm a menu selection choice in a disc's on-screen menu.

㉑ **Pause:** Press this button to pause the disc and freeze the picture during DVD or VCD playback, or to pause the playback of a CD or DVD-Audio disc. To play a DVD or VCD in the slow-forward or -reverse mode, first press this button and then press either the **Search/Slow Forward** ㉔ or **Reverse Button** ⓬.

㉒ **Zoom:** Press this button to zoom in on the image from a DVD, VCD or JPEG image. The image may be expanded by a factor of x2, x3, x4 or x5. Once the on-screen indication of the zoom ratio disappears from the screen you may use the **Navigation Buttons** ⓮ to explore the picture.

㉓ **Play:** Press this button to begin the playback of a disc, or to resume normal playback when a disc has been paused or scanned.

㉔ **Search/Slow Forward:** This button initiates fast or slow play in the forward mode. For fast forward play, each press of the button when playing DVD or VCD discs changes the speed as indicated by the number appearing in the upper right corner of the screen. For slow forward play, first press the **Pause Button** ㉑ and each subsequent press of this button will change the slow play speed as indicated by the number appearing in the upper right corner of the screen.

㉕ **Stop:** When a DVD is playing, press this button once to place the disc in the Resume mode, which means that playback will stop. However, as long as the disc drawer is not opened, playback will continue from the point where the disc was stopped when the **Play Button** ㉓ 3 is pressed again, as indicated by the LAST SCENE message (for DVDs) or the RESUME message (for CDs, MP3 files, JPEG files and VCDs with PBC) in the **Information Display** 12. Resume will not operate for WMA files or VCDs that do not have playback control. Pressing the button twice will stop the disc and play will start from the beginning of the disc when the **Play Button** ㉓ 3 is pressed again.

㉖ **Next Step/Skip:** Press this button once to advance to the beginning of the next chapter on a DVD or track on a CD. Press it again to continue to advance through the remaining chapters or tracks. After first pressing the **Pause Button** ㉑, press this button to step through a DVD-Video disc as a series of still-image frames.

㉗ **Disc Menu:** While a DVD is playing, press this button to view the disc's main menu.

㉘ **Status:** Press while a disc is playing to view the on-screen status banner display. The first press will display the current title and chapter, the play mode icon and the elapsed time, along with a "temperature

bar" display of the time elapsed. You may use the ◀▶▲▼ **Navigation Buttons** ⑭ and the **Enter Button** ⑳ to select and change the current title or chapter, or the time display. The Status Banner is only available for DVDs and VCDs when PBC is turned off. Press the button one more time to remove the status displays from the screen. More detailed information about the disc is available by pressing the **Info Button** ⑨.

㉙ **Numeric Keys:** Press these buttons to enter a number.

㉚ **Title:** When a DVD is playing, press this button to go back to the main title menu for the disc being played. If you are playing a DVD-Audio disc that contains other formats the DVD 47 is capable of playing, such as linear PCM or Dolby Digital 5.1, pressing this button may enable you to switch playback from one audio format to another.

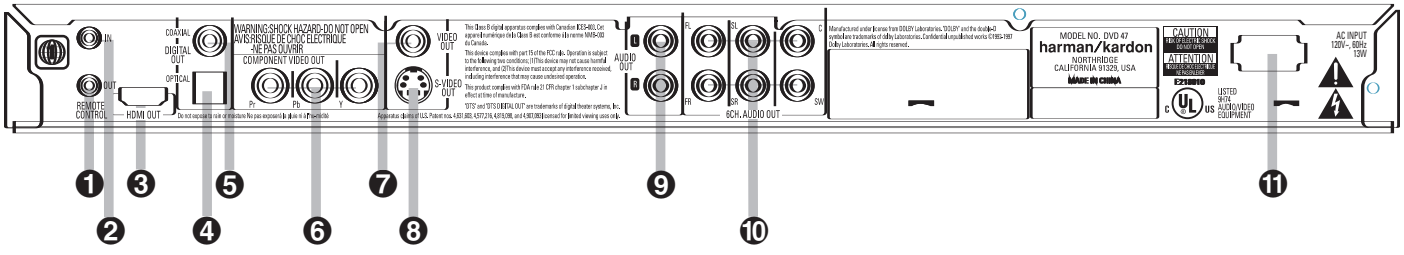
㉛ **Subtitle:** When a DVD is playing, press to select a subtitle language or to turn subtitles off.

NOTE: Due to the variations in how DVD discs are authored, the subtitle languages displayed by the DVD 47 may not accurately reflect the actual languages available on the disc. It is recommended that subtitles be selected using the disc's menu.

㉜ **Power Off:** Puts the player in Standby mode.

㉝ **IR Emitter:** This small, clear button-like device sends the IR commands from the remote control to the DVD 47. To ensure proper performance of the remote control, be sure to point it toward the unit and do not cover it with your fingers when sending remote commands.

REAR-PANEL CONNECTIONS



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

❶ Remote Control Output
❷ Remote Control Input
❸ HDMI Output
❹ Optical Digital Audio Output
❺ Coaxial Digital Audio Output
❻ Component Video Outputs
❼ Composite Video Output
❽ S-Video Output
❾ Analog Audio Outputs
❿ 6-Channel Audio Outputs
⓫ AC Power Cord

❶ Remote Control Output: Connect this jack to the infrared (IR) input jack of another compatible remote-controlled product to have the built-in Remote Sensor on the DVD 47 provide IR signals to other compatible products.

❷ Remote Control Input: Connect the output of a remote infrared sensor, or the remote control output of another compatible product, to this jack. This will enable the remote control to operate even when the front-panel Remote Sensor on the DVD 47 is blocked. This jack may also be used with compatible IR remote control-based automation systems.

❸ HDMI Output: If you have an HDMI-compatible receiver or video display device, connect this output to an HDMI input on the receiver or video display for the highest-quality uncompressed digital audio and video available. Even if your receiver is not capable of processing audio in the HDMI format, you may still experience the superb reproduction of HDMI video.

If your video display has a DVI input, you may use an optional HDMI-to-DVI cable or adapter for the connection to the display. In all cases, the video display must be HDCP-compliant in order to use the HDMI output. For best results, we do not recommend HDMI connections in excess of ten feet.

The following audio formats may be output via the HDMI connection:

Audio CD – 2-Channel PCM or 5.1-channel DTS

DVD-Audio and SACD – 2-Channel PCM

DVD-Video – Up to 5.1-channel Dolby Digital or DTS

NOTE: To hear the high-resolution surround sound recorded on DVD-Audio and SACD discs, you need to connect the **6-Channel Audio Outputs ⓾** to the corresponding input jacks on your receiver or processor. These formats are not output digitally.

❹ Optical Digital Audio Output: Connect this jack to the optical digital input of an A/V receiver or surround processor for Dolby Digital, DTS or PCM audio playback.

❺ Coaxial Digital Audio Output: Connect this jack to the coaxial digital input of an A/V receiver or surround processor for Dolby Digital, DTS or PCM audio playback.

NOTES:

- Connect either the **Optical Digital Audio Output ❹** or the **Coaxial Digital Audio Output ❺** to a corresponding digital audio input on your receiver or processor, but not both.
- The coaxial digital output should only be connected to a digital input. Even though it is the same RCA-type connector as standard analog audio connections, DO NOT connect it to a conventional analog input jack.

❻ Component Video Outputs: These outputs carry the component video signals for connection to display monitors with component video inputs. For standard analog TVs or projectors with inputs marked Y/Pr/Pb or Y/Cr/Cb, connect these outputs to the corresponding inputs. If you have a high-definition television or projector that is compatible with high-scan-rate progressive video (480p or better), connect these jacks to the HD component inputs. If you are using a progressive scan display device, PROGRESSIVE must be selected in the Video menu in order to take advantage of the progressive scan circuitry. See the "Scan Type" section on page 23 for more information on progressive scan video.

IMPORTANT: These jacks should NOT be connected to standard composite video inputs.

❼ Composite Video Output: Connect this jack to the video input on a television or video projector, or to a video input on an A/V receiver or processor if you are using that type of device for video input switching.

❽ S-Video Output: Connect this jack to the S-video input on a television or video projector, or to an S-video input on an A/V receiver or processor if you are using that type of device for S-video input switching.

❾ Analog Audio Outputs: Connect these jacks to an audio input on an A/V receiver, surround processor or your television for analog audio playback.

❿ 6-Channel Audio Outputs: Connect these outputs to the matching 6-channel analog audio inputs on your receiver or surround sound processor. This connection is required to listen to the multichannel tracks on SACD and DVD-Audio discs. If the disc also contains a linear PCM, Dolby Digital or DTS track, you may listen to it using the **HDMI ❸**, **Optical ❹** or **Coaxial Dgital Audio Output ❸** or the **Analog Audio Outputs ❾**.

⓫ AC Power Input: Plug the female end of the AC power cord included with the DVD 47 into this input, and then connect the other end of the cord to an AC outlet. If the outlet is controlled by a switch, make certain that it is in the ON position. Do not substitute another power cord for the one provided with the DVD 47. If the cord becomes damaged, contact your authorized Harman Kardon dealer for a replacement.

NOTE: You'll find more details about all audio/video connections under Setup and Connections on the following pages.

- Ensure that the power switch of this unit (and of other equipment to be connected) is set to "Off" before commencing connection. We also strongly recommend that you leave all system components unplugged from AC power until after you have completed the interconnections described in this section.
- Do not block the ventilation holes of any of the equipment and arrange them so that air can circulate freely.
- Read through the instructions before connecting other equipment.
- Ensure that you observe the color-coding when connecting audio and video cables.

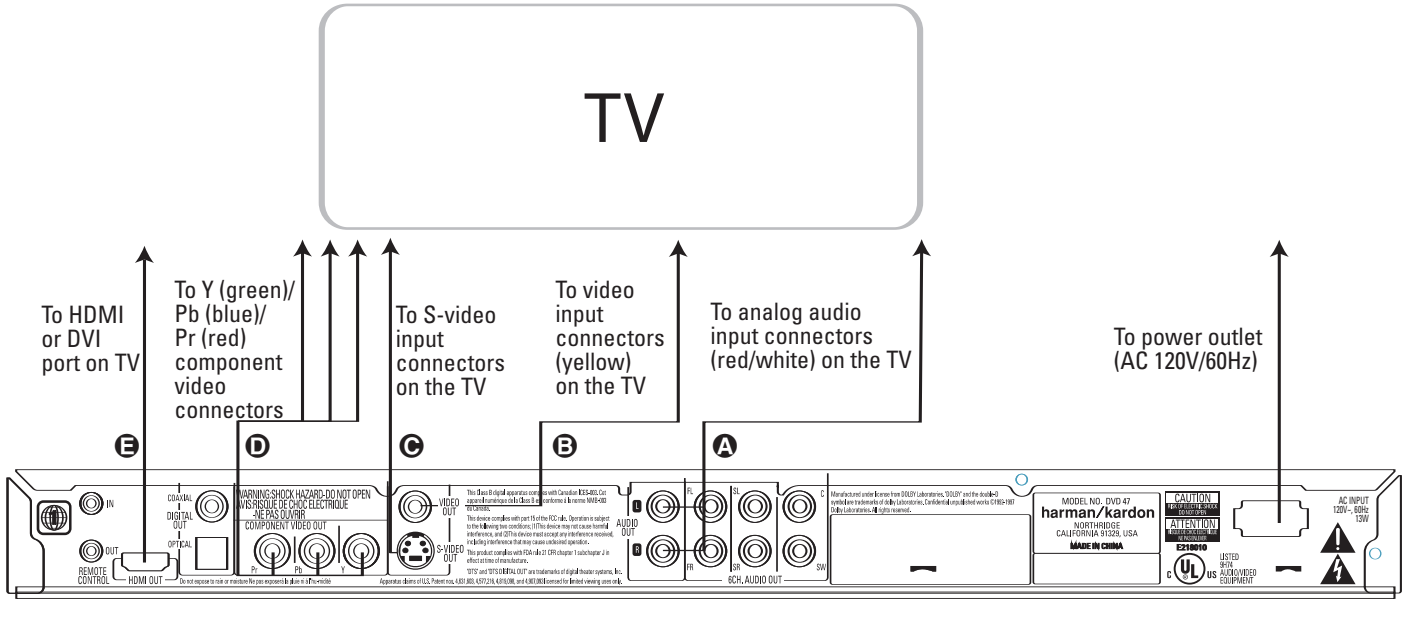
VIDEO NOTES:

- For the best quality, if your receiver or processor and/or video display are HDMI-capable, we recommend using the HDMI output. With a single cable connection between components, HDMI is able to deliver uncompressed high-definition digital video and digital audio programming. Even without audio processing capability, your HDMI-ready receiver will be able to pass the uncompressed digital video signal to your video display.

  NOTE: If your video display has a DVI input, you may use an optional HDMI-to-DVI cable or adapter for the connection to the display. In all cases, the video display must be HDCP-compliant in order to use the HDMI output.
- If your equipment is not HDMI-ready, we recommend the use of component video for higher quality pictures. You may also use the standard S-video or composite video connection if your TV does not have component video inputs. The component and S-video outputs are not available simultaneously.
- The composite video output (yellow) sends the complete video signal to the TV (or to the A/V receiver) by one cable only. Use this video output when your TV set is equipped with a video input jack only.
- The S (separate) video output connector separates the color (C) and luminance (Y) signals before transmitting them to the TV set in order to achieve a sharper picture. Use the S-video cable when connecting the player to a TV equipped with an S-video input for improved picture clarity.
- The component video outputs further separate the color components of the video signal, optimizing the DVD 47's video performance. Component video connections are preferred, when available on your TV or receiver. If you are using a television or video display that is compatible with high-resolution 480P video signals, make sure to use the input jacks on the video display marked "HD Component," if available. Also, make sure to configure the display's input settings for use with "480P" video signals. You will also need to change the scan type in the DVD 47's Video Setup menu from "Interlaced" to "Progressive." See page 23.
- Modern audio/video receivers are capable of connection to several video source devices, such as the DVD 47 and a VCR, cable television set-top box, HDTV tuner or other device. The receiver is equipped with video monitor outputs for connection to your television, projector or plasma display. As you select any input source device, the receiver selects the correct video input and routes it to the correct video monitor output to your television. It is recommended that you connect one of the video outputs from the DVD 47 to the corresponding input on your receiver to simplify operation of your home entertainment system. Refer to the owner's guide for your receiver for more information.
- If your receiver is capable of multiroom operation, it is recommended that you connect both the component (or HDMI) and composite video outputs of the DVD 47 to the receiver. This enables the highest-quality picture (component video) for viewing in the main listening room, while enabling the multiroom system, if it is video-capable, to distribute the composite video signal to the remote zone. Consult the owner's guide for your receiver to determine whether it has video multiroom capability.

Connecting to a TV Only

When using the DVD 47 with a television but no audio receiver or processor, connect it as follows. Make the **Analog Audio Connection** Ⓐ and one of the **Video Connections** (**Composite Video** Ⓑ, **S-Video** Ⓒ, **Component Video** Ⓓ). If your television or video display is HDMI-capable, you only need to make the **HDMI** Ⓔ connection, as it handles both audio and video. Remember to plug in the power cord.



SETUP AND CONNECTIONS

Connecting to a Receiver/Amplifier With a Dolby Digital or DTS Decoder

One of the major advantages of the DVD format is its ability to use a variety of digital audio formats for the ultimate in sonic performance. However, in order to enjoy the benefits of digital audio, you must use a receiver or processor that has digital audio decoding capabilities and make an optical or coaxial digital audio connection between the DVD 47 and your home theater system. This simple connection is made as shown below with an optional coax or optical cable. Only one of these connections is required, and both should not be made at the same time.

In order to take advantage of the high-resolution SACD and DVD-Audio output of the DVD 47, you must connect the **6-Channel Audio Outputs ⑩** to the matching 6-channel inputs on your receiver or processor. Only compressed PCM, Dolby Digital or DTS tracks that may be present on the disc may be listened to using the digital audio outputs. Thus, the DVD 47 decodes the digital signal and outputs separate signals for each channel: front left, center, front right, surround right, surround left and low-frequency effects (LFE).

NOTES FOR ANALOG AUDIO:

- If you wish to use the DVD 47 as the input for a multiroom system, the **Analog Audio Outputs ⑨** should be connected to the standard analog left/right DVD or CD inputs on your digital receiver or processor.
- The connection from the **Analog Audio Outputs ⑨** to the TV is optional. If you plan on occasionally using your DVD 47 alone, without turning on your complete system, this connection must be made.
- When the audio signal is to be fed to an analog receiver rather than to the TV, connect the **Analog Audio Outputs ⑨** to any analog audio inputs on your receiver or processor. The DVD 47 will "downmix" multichannel recordings to two channels.
- The analog audio connection should also be made if you wish to play high-resolution 96kHz PCM audio discs where your receiver does not support 96kHz processing.

NOTES ON VIDEO:

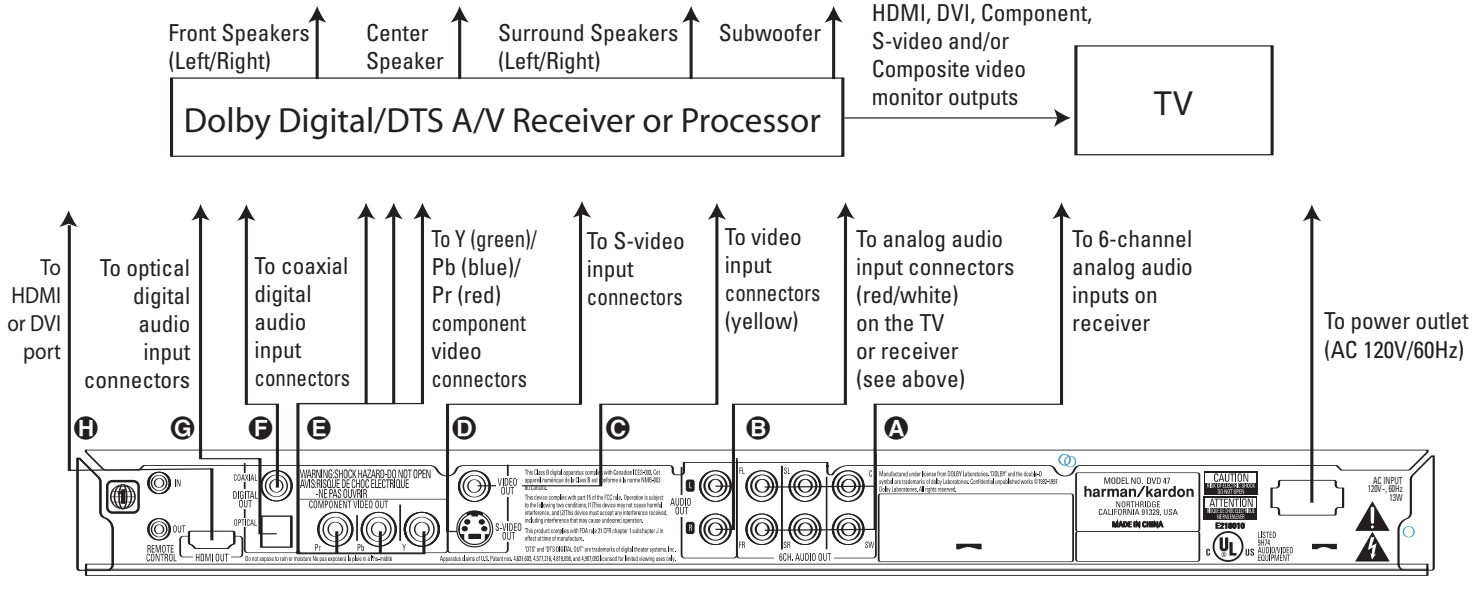
- With multiple video sources, your audio/video receiver can be used for selecting the video signal and routing it to the TV. Connect the **HDMI ❸**, **Component ❺**, **Composite ❻** or **S-Video ❼** output of the DVD 47 to the correct video input on your receiver, and the video outputs of the receiver to your TV. For more details, see the manual for your audio/video receiver.
- If your receiver has only DVI inputs, you may use an optional HDMI-to-DVI cable or adapter for the connection to the receiver. In addition, the video display used with your system must be HDCP-compatible in order to take advantage of the HDMI output, whether it is used with HDMI or DVI connections.

Connecting to a Receiver

When using the DVD 47 with an audio/video receiver or processor, connect it as follows. First, make one of the video connections (**Composite Video Ⓒ**, **S-Video Ⓓ**, **Component Video Ⓔ** or **HDMI Ⓗ**) to the video input jacks on the A/V receiver, and then connect the receiver's video monitor output to the TV. If you will sometimes use the TV without the audio component, you may optionally make the **Analog Audio Connection Ⓑ** to the TV. In addition, to benefit from the high-resolution surround sound formats recorded on SACD and DVD-Audio discs, which are not output via the HDMI connection, you will need to make the **6-Channel Audio Connection Ⓐ** to your receiver or processor.

Second, if your receiver or processor is not HDMI-capable, make either the **Optical Digital Audio Connection Ⓖ** or the **Coaxial Digital Audio Connection Ⓕ**, to the receiver or processor. Remember that when the HDMI connection is used with a receiver or processor that is compliant with the HDMI format, a single connection suffices for both audio and video, except for SACD and DVD-Audio discs, as noted. If your receiver or processor is not capable of processing the HDMI audio signal, then a separate audio connection is required. If your receiver/processor has multiroom capability, you may also connect the DVD 47's analog audio outputs to the DVD analog audio inputs on the receiver.

IMPORTANT NOTE: Make certain that any device being connected, including the DVD 47, your receiver or processor and your TV or video display, is turned off whenever you make connections between products.



TEST SCREEN

DVD is one of the highest quality sources ever made available for in-home playback of prerecorded pictures and sound. In order to make certain that your home theater system is fully optimized to take advantage of DVD's superb picture quality, the DVD 47 offers a built-in video test signal that makes it easy to calibrate your TV or video display for proper playback.

Test Screen

With the test screen showing on your video display, the following adjustments may be made:

- The proper color intensity setting on your TV.
- Proper color adjustments using the color bars, which should be (left to right) black, white, yellow, cyan (turquoise), green, magenta, red, blue, black.
- The proper color transition, seen as sharp separation of the bars.
- The performance of the color circuits in your TV (with "Video" signals); bar edges should show no vertical crawling dots.

With the gray scale and the black/white fields below the color bars, the brightness and contrast of your screen can be adjusted.

NOTE: Most of the video adjustments using the DVD 47's test screen should be made using the controls on your video display, with the DVD 47's controls set at their factory default position in the center. If necessary, you may tweak the brightness and sharpness using the controls found in the DVD 47's video adjustments menu.

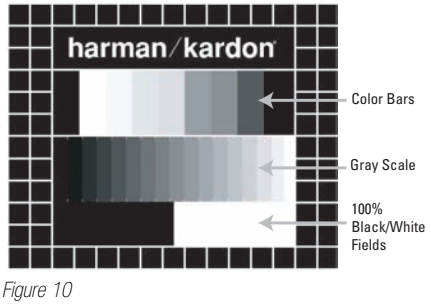


Figure 10

TV Picture Adjustment With Test Screen

Brightness Adjustment:

1. Turn down the color control on your TV until the color bars are visible in black and white.
2. Adjust the contrast on your TV to the lowest level where you still can see all bars within the gray scale in the test picture separately and clearly.
3. Adjust the brightness using the DVD 47 video adjustments control so that the bars in the gray scale are all visible. The bar furthest to the left has to be as black as possible rather than gray, but the next gradation must clearly be distinct from it. All the bars in the gray scale should be gradually and evenly changing from black to white, going from left to right.

Contrast Adjustment:

1. Adjust the contrast on your TV until you see a bright white bar in the lower right corner of the screen and a deep-dark-black bar to the left. The optimal contrast setting will depend on your preference and the surrounding light in the TV room.
2. If the brightness of the white bar no longer increases when the contrast is turned up or the borders of the white "harman/kardon" letters on top bloom (overlight) into the black areas (drastically decreasing the sharpness of the type), the contrast has been turned up too much. Reduce the contrast until these effects disappear and the video still looks realistic.
3. If you are watching TV with customary surrounding daylight, adjust the contrast so that a normal video picture has about the same look as the surroundings in your room. That way the eye is relaxed when watching the TV picture. This contrast setting may be reduced when the surrounding light is dimmed, thereby usually improving the sharpness of a video significantly.
4. The gray scale in the middle line needs to have the same clear difference between each bar as before the contrast adjustment. If not, go back to "Brightness Adjustment" and repeat Step 3 and then "Contrast Adjustment," making only minor adjustments each time for optimization.

Color Adjustment

1. When the brightness and contrast are set optimally, turn up the color control to the level of your preference. Adjust to the level where the colors look strong but still natural, not overdone. If the color level is too high, depending on the TV, some of the bars will seem wider or the color intensity will not increase while the control is turned up. Then the color control must be reduced again. Ultimately, you also should test the color intensity with a video – e.g., pictures of natural faces, flowers, fruit and vegetables, and other common natural articles for an optimal setting of the color intensity.
2. Use the large white bar below the gray scale to tweak the warmth of the picture. Every viewer has a preference as to how the glow of the picture should be. Some prefer a little colder picture, some a warmer glow. The Tint function on your TV and the white bar can be used to control this. Adjust the Tint to the level where you feel the white color has the tone you prefer.

Sharpness Adjustment

Contrary to intuition, the picture will appear sharper and clearer with the sharpness, or Edges, setting backed off from the maximum setting. Reduce the sharpness setting on your television, and the Edges setting on the DVD 47 video adjustments menu if necessary, to minimize the appearance of any white lines between the bars in the gray scale portion of the test screen.

Convergence and Edge Focus

The crosshatch pattern that surrounds the test screen may be used to evaluate edge focus and convergence in front- or rear-projection video displays. However, the controls used to adjust these parameters are often not user-accessible. In any event, these adjustments are extremely complex, and require proper training and experience to avoid worsening the situation. Therefore, it is recommended that if you are unable to improve the picture using the available controls, contact the video display manufacturer's authorized service representative for assistance.

When all desired setup and configuration entries have been made, use the ▲▼ Navigation Buttons ⑭ until "Done" is highlighted at the bottom of the Video Adjustments submenu. Press the Enter Button ⑳ to select it to return to the on-screen menu system. Then, press the Setup Button ⑩ to remove the menu displays from the screen. The unit will return to normal operation and you are ready to enjoy the finest in DVD or CD playback!

PLAYBACK BASICS

Loading Discs

To load discs in the DVD 47, first turn the DVD 47 on by pressing in the **Power On/Off Switch** 2 or **Power On Button** 1. Note that the **Power Indicator** 1 will turn amber when the unit is connected to an AC power source. It will turn blue when the **Power On Button** 2 1 is pressed.

Next, press the **Open/Close Button** 2 11 until the disc tray opens.

Hold the disc by the edge, and gently place it into the disc drawer, making certain that the disc is properly seated in the tray's insert. If the disc is not correctly centered, you may damage both the disc and the player when the drawer closes. When loading discs, please note the following:

- The DVD 47 will play discs with the following logos as well as most DVD-RW or DVD+RW discs and most WMA and JPEG discs, including Kodak Picture CDs, but not Kodak Photo CDs. DO NOT attempt to play another type of disc.

- The DVD 47 will only display video in the NTSC format. Although the PAL format is generally used in Europe and other regions of the world outside North America, some music or other DVDs are available in PAL with a Region Code of "0," which means they may be played on any DVD player around the world. The DVD 47 will automatically detect the PAL format, and make the necessary conversions so that the video may be displayed on an NTSC TV. PAL discs bearing a Region Code other than "0" or "1" may not be played on the DVD 47.
- Playback capability for CD-RW, DVD-RW, DVD-R, DVD+RW or DVD+R discs will vary according to the quality of the disc. On some occasions it is possible that these discs may not play on the DVD 47. This does not indicate any problem with the DVD 47.
- The DVD 47 will only play discs that are coded for Region 1 or discs that are open to being played in all regions (Region Code "0"). Discs that contain a Region Code of 2, 3, 4, 5 or 6 (as noted by a number inside a world map logo on the disc's cover jacket or case) will not play.
- Both 5-inch (12cm) and 3-inch (8cm) discs may be used.
- When loading CDs, SACDs or DVD-Audio discs, load the discs with the label side up.
- When loading DVD-Video discs with printed labels, load them label side up.
- Some DVD-Video discs are double-sided. The title information for these will be printed on the inner ring of the disc, very close to the center hole. The title for the side you wish to play should be facing up.

After a disc is properly loaded, press the **Open/Close Button** 2 11 to close the disc drawer. After the drawer closes, you will see a brief indication of LOADING in both the **Main Information Display** 12 and in the on-screen display to alert you to the fact that the unit is determining the type of disc (DVD-Video, DVD-Audio, SACD, CD, VCD, JPEG, WMA or MP3) and is reading the data for track, chapter, title and other information about the disc.

Once the disc's data has been read, the type of disc will be displayed by the **Disc-Type Indicator** A and its type will be identified in the upper right corner of the screen. If the disc is a DVD, SACD, CD or VCD2.0 disc, it will automatically begin playing. The disc's track timing information and other relevant data will appear in the **Main Information Display** 12.

Any time a control button is pressed, an icon will appear in the upper right corner of the screen to indicate the player's action. These icons include the standard transport modes (play, stop, pause, forward and reverse fast and slow search, track skip), the open/close disc drawer symbol, the repeat and random modes, and the prohibit icon (Ø) if the command action is not available at that time or for that disc. As explained in more detail in other sections of this manual, pressing the **Status Button** 28 displays the Status Banner for DVDs, and pressing the **Info Button** 9 displays the Player Information menu.

- When a DVD is detected, playback will automatically begin and the screen will show the program or the disc's menu, depending on how the disc was created.
- If a CD is detected, playback will begin automatically.
- If the disc contains MP3, WMA or JPEG files, or if it is a VCD without playback control, the Player Information display will appear (see Figure 11). To play one of these files, you may need to use the ▲▼◀▶ **Navigation Buttons** 14 to select a folder and press the **Enter Button** 20 to open it. Use the ▲▼ **Navigation Buttons** 14 to select a file for playback, and press the **Enter Button** 20 to begin play.
- VCD2.0 discs will begin play automatically, similar to a conventional audio CD.

Figure 11

If a disc is already in the drawer when the unit is turned on, it will begin playing. If the disc was stopped using the Resume function, playback will begin from the point where it was stopped. If the disc was stopped by pressing the **Stop Button** 5 25 twice, the disc will begin playing from its beginning.

Playback Features for DVD and CD Discs:

- To momentarily pause playback and freeze the current picture frame on a DVD, press the **Pause Button** 4 21. To resume playback after pressing the Pause button, press the **Play Button** 3 23.
- To move forward or backward through the tracks on a DVD-Audio disc or CD, or the chapters on a DVD, press the **Skip Forward/Reverse Buttons** 6 7 on the front panel or the **Previous/Next Buttons** 11 26 on the remote.
- To move forward or backward through the DVD or CD disc being played at fast speed, press the **Search Forward/Reverse Buttons** 12 24, or press and hold the front-panel **Skip/Search Buttons** 6 7 briefly until fast play begins, and then release them. Once one of these buttons is pressed, the fast search will continue until the **Play Button** 3 23 is pressed. Each press of the **Search Forward/Reverse Buttons** 6 7 12 24 will cycle to the next speed in the following order: 2x, 4x, 8x, 20x, 100x.

NOTE: Fast search is available when DVD-Audio, SACD and MP3 discs are playing, but not for WMA files.

- When a DVD is playing, you may move forward or backward through the disc in slow motion by first pressing the **Pause Button** 4 21 and then pressing the **Search/Slow Forward** or **Search/Slow Reverse Buttons** 6 7 12 24. Each press of the buttons will cycle the player through one of the four forward slow-play speeds: 1/2x, 1/4x, 1/8x or 1/16x or one of the two reverse slow-play speeds: 1/2x or 1/4x. Press the **Play Button** 3 23 to resume normal playback.

Note that there is no audio playback during fast or slow-forward or -reverse play. This is normal for DVD, as A/V receivers and surround processors cannot

process the digital audio streams during slow modes. Slow-play is not available for CD discs.

- To advance frame by frame while a DVD is playing, first press the **Pause Button** 4 21, then press the **Skip/Step (Previous)** 6 11 or **Skip/Step (Next)** 7 26 buttons repeatedly. Press the **Pause** 4 21 or **Play Button** 3 23 to resume normal play. Frame-by-frame movement in reverse is not available.
- When a camera icon shows on the screen, or the **Angle Indicator** E appears, this is your indication that there is multiple-angle information on the disc being played. To change the angle, press the **Angle Button** 13 repeatedly until the desired angle view appears. An on-screen banner message will appear to indicate the angle view in use.

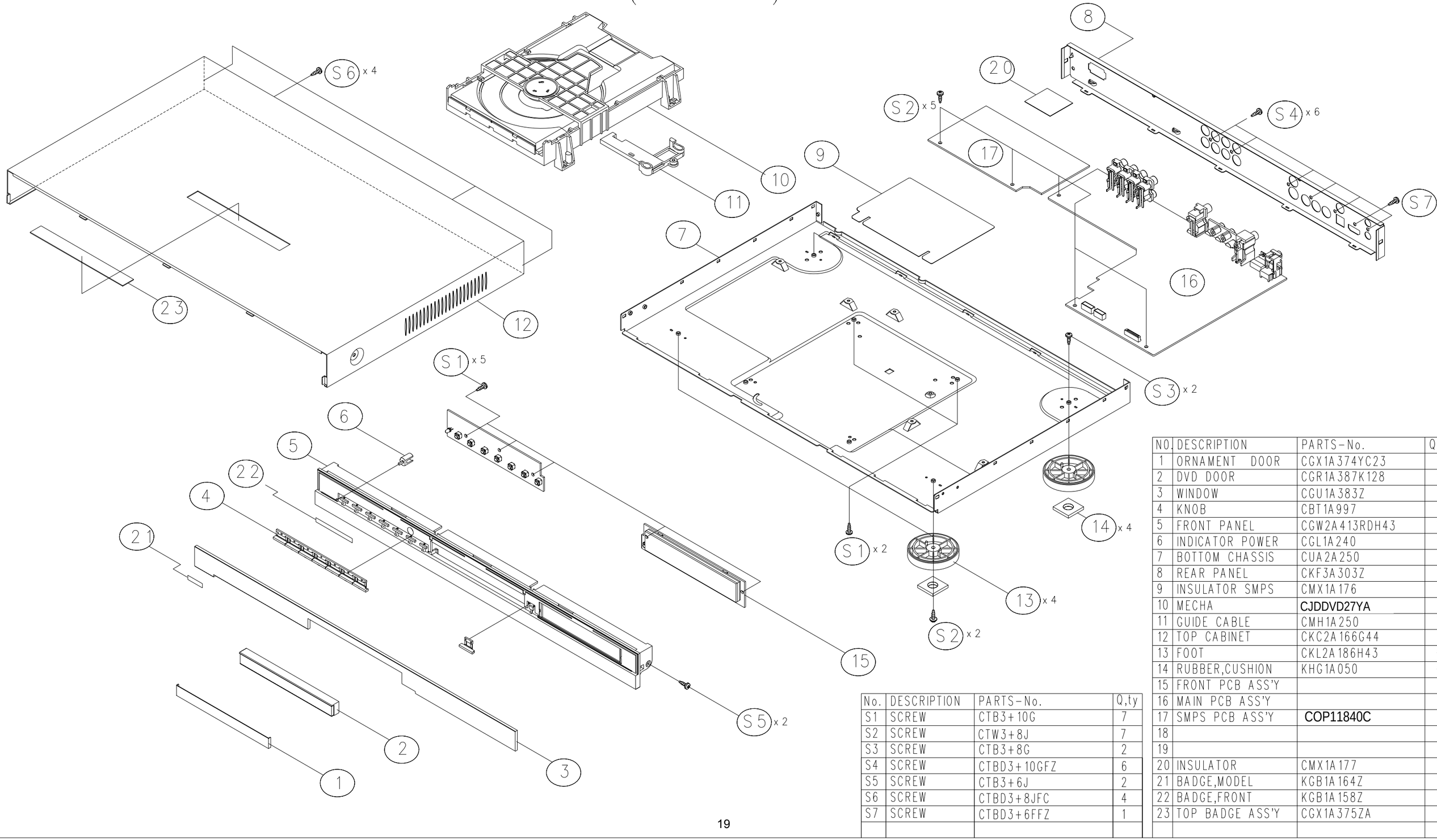
To illuminate the buttons on the remote control so that they may be seen in low-light conditions, press the **Light Button** 15.

TROUBLESHOOTING GUIDE

TROUBLESHOOTING GUIDE

SYMPTOM	POSSIBLE CAUSE	SOLUTION
Unit does not turn on	• No AC power	• Check AC power plug and make certain any switched outlet is turned on.
Disc does not play	• Disc loaded improperly	• Load disc label-side up; align the disc with the guides and place it in its proper position.
	• Incorrect disc type	• Check to see that disc is SACD, CD, CD-R, CD-RW, VCD, MP3, WMA, JPEG, DVD-R, DVD-RW, DVD+R, DVD+RW (standard-conforming), DVD-Audio or DVD-Video; other types will not play.
	• Invalid Region Code	• Use Region 1 or Open Region (0) disc only.
	• Rating is above parental preset	• Enter password to override or change rating settings (see page 20).
No picture	• Intermittent connections	• Check all video connections.
	• Wrong input	• Check input selection of TV or receiver.
	• Progressive Scan output selected	• Use Progressive Scan mode only with compatible TV. Press **Progressive Scan/ Interlaced Button** ⑲ to toggle to the correct mode (see page 23).
	• Video Off feature active	• Press **Video Off Button** ⑯ to reactivate video circuitry.
	• **HDMI Output** ❸ is connected to a video display that is not HDCP-compliant.	• The **HDMI Output** ❸ may not be used with video displays that are not HDCP-compliant. Unplug the cable and select another audio and video connection (see pages 14 through 16).
No sound	• Intermittent connections	• Check all audio connections.
	• Incorrect digital audio selection	• Check digital audio settings on DVD 47 and on receiver.
	• DVD disc is in fast or slow mode	• There is no audio playback on DVD discs during fast or slow modes.
	• Surround receiver not compatible with 96kHz PCM audio	• Use analog audio outputs.
	• DVD Audio or SACD disc is loaded without using analog audio connection	• Use **6-Channel Audio Outputs** ⑩ or **Analog Audio Outputs** ❾.
Picture is distorted or jumps during fast forward or reverse play	• MPEG-2 decoding	• It is a normal artifact of DVD playback for pictures to jump or show some distortion during rapid play.
Some remote buttons do not operate during DVD play; prohibited symbol ⃠ appears (see below)	• Function not permitted at this time	• With most discs, some functions are not permitted at certain times (e.g., Track Skip) or at all (e.g., direct audio track selection).
The OSD menu is in a foreign language	• Incorrect OSD language	• Change the display language selection (see page 23).
The ⃠ symbol appears	• Requested function not available at this time	• Certain functions may be disabled by the DVD itself during passages of a disc.
Picture is displayed in the wrong aspect ratio	• Incorrect match of aspect ratio settings to disc	• Change aspect ratio settings (see page 23).
Remote control inoperative	• Weak batteries	• Change both batteries.
	• Sensor is blocked	• Clear path to sensor or use optional outboard remote sensor.
Disc will not copy to VCR	• Copy protection	• Many DVDs are encoded with copy protection to prevent copying to VCR.
Password not accepted.	• Incorrect password being used or password has been forgotten.	• Stop play of disc. Press and hold **Clear Button** ❹ until the display blinks. This resets the password and all settings to their defaults.

EXPLODED VIEW(DVD47)



No.	DESCRIPTION	PARTS-No.	Q,ty
S1	SCREW	CTB3+10G	7
S2	SCREW	CTW3+8J	7
S3	SCREW	CTB3+8G	2
S4	SCREW	CTBD3+10GFZ	6
S5	SCREW	CTB3+6J	2
S6	SCREW	CTBD3+8JFC	4
S7	SCREW	CTBD3+6FFZ	1

NO.	DESCRIPTION	PARTS-No.	Q,ty
1	ORNAMENT DOOR	CGX1A374YC23	1
2	DVD DOOR	CGR1A387K128	1
3	WINDOW	CGU1A383Z	1
4	KNOB	CBT1A997	1
5	FRONT PANEL	CGW2A413RDH43	1
6	INDICATOR POWER	CGL1A240	1
7	BOTTOM CHASSIS	CUA2A250	1
8	REAR PANEL	CKF3A303Z	1
9	INSULATOR SMPS	CMX1A176	1
10	MECHA	CJDDVD27YA	1
11	GUIDE CABLE	CMH1A250	1
12	TOP CABINET	CKC2A166G44	1
13	FOOT	CKL2A186H43	4
14	RUBBER,CUSHION	KHG1A050	4
15	FRONT PCB ASS'Y		1
16	MAIN PCB ASS'Y		1
17	SMPS PCB ASS'Y	COP11840C	1
18			1
19			1
20	INSULATOR	CMX1A177	1
21	BADGE,MODEL	KGB1A164Z	1
22	BADGE,FRONT	KGB1A158Z	1
23	TOP BADGE ASS'Y	CGX1A375ZA	1

DISASSEMBLY PROCEDURES (DVD27)

<1> TOP-COVER (21) REMOVAL

1. Remove 4 screws and then remove the Top-cover.

<2> FRONT PANEL ASS'Y REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the lead wire (BN72-32p) on the Fip PCB (37-1) from connector (CN72) on the Input PCB (39-1)
3. Disconnect the lead wire (BN80-11P) on the Fip PCB (37-1) from connector (CN80) on the Main PCB (38-1).
4. Disconnect the lead wire (BN16-6P) on the Tone PCB (37-3) from connector (CN16) on the Connect PCB (37-7).
5. Disconnect the lead wire (BN41-6P) on the Tone PCB (37-3) from connector (CN41) on the Video PCB (40-1).
6. Disconnect the lead wire (BN18-5P) on the Digital input PCB (37-8) from connector (CN18) on the Input PCB (39-1).
7. Disconnect the lead wire (BN81-8P) on the Fip PCB (37-1) from connector (CN81) on the Trans PCB (40-5).
8. Disconnect the lead wire (BN15-8P) on the Fip PCB (37-1) from connector (CN15) on the Download PCB (37-9).
9. Remove 1 screw(S10) and then lead wire (JW82-2P) on the Phone PCB (37-4).
10. Remove 1screw(S10) and then lead wire (JW84-1P) on the Tone PCB (37-3)
10. Remove 10 screws (S1) and then remove the Front Panel ASS'Y.

<3> TONE PCB (37-3) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Front Panel ASS'Y, referring to the previous step<2>.
3. Pull out the Volume Knob ASS'Y & 3 Rotary Knobs (5).
4. Remove 10 screws (S2,S14), and then remove the Tone PCB (37-3).
5. Disconnect the lead wire (BN84-5P) One the Tone PCB (37-3) from connector (CN84) on the Fip PCB (37-1)

<4>PHONE PCB (37-4) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Front Panel ASS'Y, referring to the previous step<2>.
3. Disconnect the lead wire (BN85-2P) on the Fip PCB (37-1) from connector (CN85) on the Phone PCB (37-4)
4. Remove 2 screws (S2,S3) and then remove the Phone PCB (37-4)

.

<5>POWER LED PCB (37-6) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Front Panel ASS'Y, referring to the previous step<2>.
3. Remove 2 screws (S2) and then remove the Power led PCB (37-6).
4. Disconnect the lead wire (CN88) from connector (BN88-4P) on the Fip PCB (37-1).

<6>FIP PCB (37-1) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Front Panel ASS'Y, referring to the previous step<2>.
3. Remove the Tone PCB (37-3), referring to the previous step<3>.
4. Remove the Phone PCB (37-4), referring to the previous step<4>.
5. Remove the Power led PCB (37-6), referring to the previous step<5>.
6. Remove 6 screws (S2) and then remove the Fip PCB (37-1)

<7>TUNER MODULE (42) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the connector (CON1-Card cable) from connector (CN13) on the Input PCB ASS'Y(39-1).
3. Remove 2 screws (S8) and then remove the Tuner Module (42).

<8>VIDEO PCB (40-1) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the lead wire (BN41-6P) on the Tone PCB (37-3) from connector (CN41) on the Video PCB (40-1
3. Disconnect the connector (CN15-Card cable) on the Input PCB (39-1) from connector (CN43) on the Video PCB (40-1).
4. Remove 6 screws (S8) and then remove the Video PCB (40-1).

<9>I-POD PCB (41) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the lead wire (BN42-5P) on the INPUT PCB (39-1) from connector (CN42) on the I-POD PCB (41).
3. Disconnect the lead wire (BN45-4P) on the INPUT PCB (39-1) from connector (CN45) on the I-POD PCB (41).
4. Disconnect the lead wire (BN44-4P) on the Download PCB (37-9) from connector (CN42) on the I-POD PCB (41).
5. Remove 2 screws (S13) and then remove the I-POD PCB (41).

<10>INPUT PCB (39-1) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Connect PCB (37-7).
3. Disconnect the lead wire (BN18-5P) on the Digital input PCB (37-8) from connector (CN18) on the Input PCB (39-1).
4. Disconnect the connect (BN72-Card canle)) on the Fip PCB (37-1) from connector (CN72) on the Input PCB (39-1)
5. Remove 11 screws (S8,S11) and then remove the Input PCB (39-1).

<11>Download PCB (37-9) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the connector (CN15) from lead wire (BN15-8P) on the Fip PCB (37-2)
3. Remove 2 screws (S4) and then remove the Download PCB (37-9).

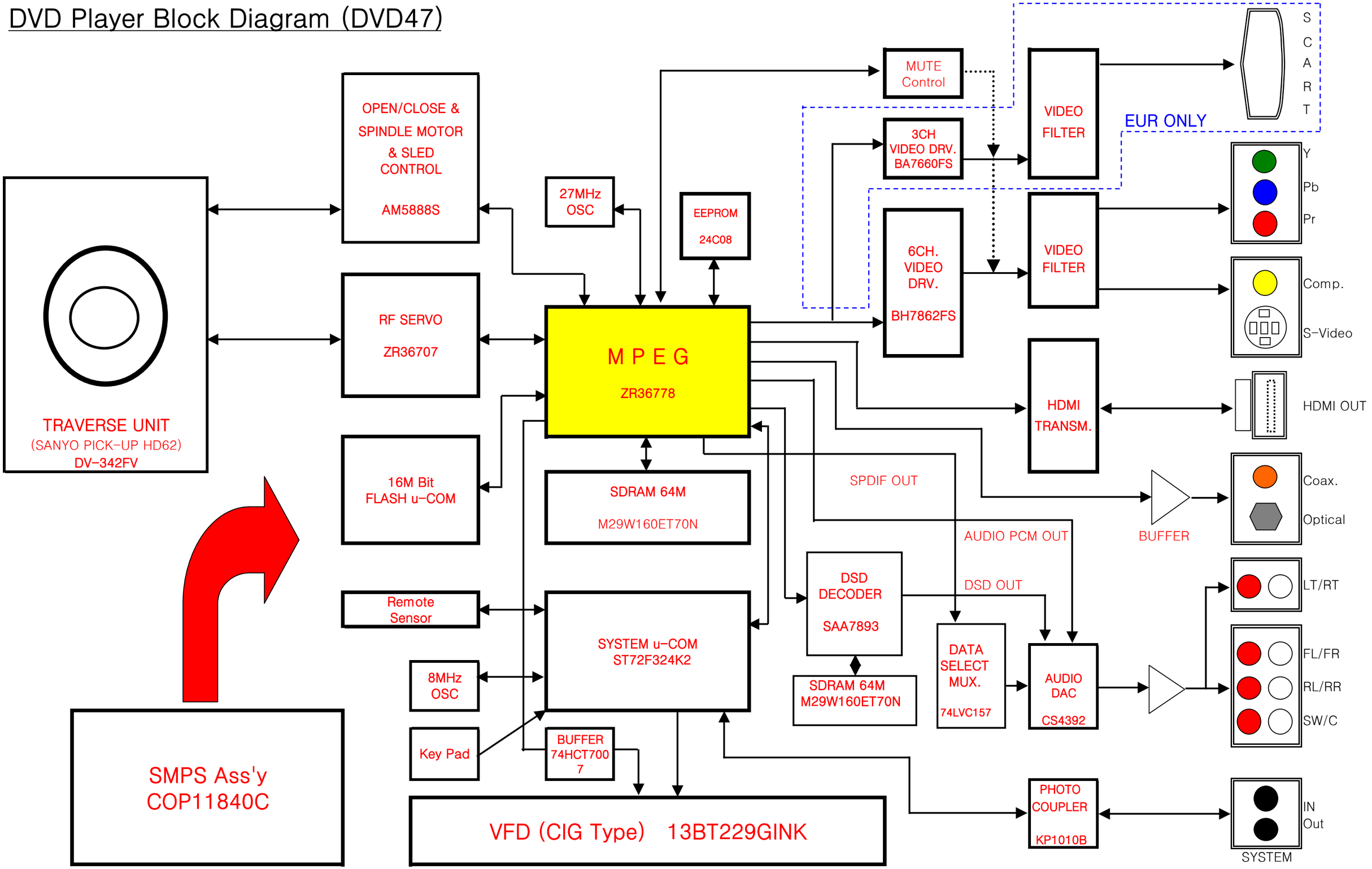
<12>POWER TRANS (36) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Disconnect the connector (BN20,BN96) on the Trans PCB (40-4) from lead wire (CN20-3P,CN96-6P) on the Main PCB (38-1).
3. Remove 4 Trans screws (S9) and then remove the Power Trans (36).

<13>MAIN PCB ASS'Y (38-1) REMOVAL

1. Remove the Top-cover, referring to the previous step<1>.
2. Remove the Tuner module, referring to the previous step<7>.
3. Remove the Video PCB, referring to the previous step<8>.
4. Remove the Input PCB, referring to the previous step<9>.
5. Disconnect the connector (CN80) from lead wire (BN80-11P) on the Fip PCB (37-1).
6. Disconnect the connector (CN91) from lead wire (BN91-3P) on the Moms PCB (37-5).
7. Disconnect the connector (CN20,BN96) from lead wire (CN20-3P,BN96-8P) on the Trans PCB (40-4,40-5)
8. Remove 11screws (S1-1EA, S4-2EA, S6-2EA, S8-6EA) and then remove the Main PCB ASS'Y(38-1).

DVD Player Block Diagram (DVD47)



DVD47 Electrical Parts List				
Ref. Designator	Part Number	Description		Qty
SMPS PCB ASS'Y				
Capacitors				
C905	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF	1
C906	CCKT1H331KB	CAP , CERAMIC	330PF 50V KB	1
C907	CCEA1HH100T	CAP , ELECT	10UF 50V	1
C908	CCEA1HH470T	CAP , ELECT	47UF 50V	1
C910	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1
C921	CCEA1EH331T	CAP , ELECT	33OUF 25V	1
C922	CCEA1HH0R1T	CAP , ELECT	0.1UF 50V	1
C923	CCEA1EH331T	CAP , ELECT	33OUF 25V	1
C924	CCEA1VH101T	CAP , ELECT	100UF 35V	1
C925	CCEA1EH331T	CAP , ELECT	33OUF 25V	1
C926	HCQI1H102JZT	CAP , MYLAR	1000PF 50V J	1
C927	CCEA1HH470T	CAP , ELECT	47UF 50V	1
C928	CCEA1HH470T	CAP , ELECT	47UF 50V	1
C929	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF	1
C931	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF	1
C935	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF	1
C901	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	0.1UF	1
C902	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	0.1UF	1
C903	CCET400VKRH470K	CAP , ELECT(400V/47uF)	KOSHIN KRH SERI	1
C904	CCKT3A222KBL	CAP , CERAMIC	EKR3A222K05FK5	1
C920	CCEA1EH102T	CAP , ELECT	1000UF 25V	1
C930	CCKDHS222ME	CAP , CERAMIC (400V Y-CAP)	SDE2G222M10FF7	1
C932	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	SDE2G102M10FF7	1
C933	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	SDE2G102M10FF7	1
Semiconductors				
D906	HVDMTZJ12BT	DIODE , ZENER 12V	MTZJ12B 1/2W	1
D907	HVD1N4148T	DIODE	1N4148	1
D909	HVDMTZJ24BT	DIODE , ZENER 24V	MTZJ24BT 1/2W	1
D910	HVD1N4148T	DIODE	1N4148	1
D911	HVD1N4148T	DIODE	1N4148	1
D912	HVDMTZJ5.1BT	DIODE , ZENER 5.1V	MTZJ5.1B 1/2W	1
D925	HVD1N4148T	DIODE	1N4148	1
D926	HVDMTZJ12BT	DIODE , ZENER 12V	MTZJ12B 1/2W	1
D928	HVDMTZJ2.7BT	DIODE , ZENER 2.7V	MTZJ2.7B 1/2W	1
IC92	HVIKIA431BAT	I.C , REGULATOR	KIA431B	1
Q904	HVTKTC3198YT	TRANSISTOR NPN	KTC3198Y	1
Q905	HVTKTA1273YT	TR NORMAL KTA1273/PNP/TO-92L	KTA1273Y	1
Q906	HVTKSC1008YT	TRANSISTOR NPN	KSC1008Y	1
Q907	HVTKRC102MT	TRANSISTOR PNP	KRC102M	1
Q908	HVTKRA102MT	TRANSISTOR PNP	KRA102M	1
Q910	HVTKSC1008YT	TRANSISTOR NPN	KSC1008Y	1
Q911	HVTKSA708YT	TRANSISTOR PNP	KSA708Y	1
Q912	HVDMCR100-6ZL1G	SCR (ON SEMI)	DMCR100-6ZL1G	1
D901	HVD1N4007T	DIODE	1N4007 (1000V/1A)	1
D902	HVD1N4007T	DIODE	1N4007 (1000V/1A)	1
D903	HVD1N4007T	DIODE	1N4007 (1000V/1A)	1
D904	HVD1N4007T	DIODE	1N4007 (1000V/1A)	1
D905	HVDUF4007T	DIODE , SCHOTTKY	UF4007	1
D908	HVD1N4007T	DIODE	1N4007 (1000V/1A)	1
D913	HVD1N4148T	DIODE	1N4148	1
D920	HVD31DQ06H	DIODE	31DQ06-FC5	1

Ref. Designator	Part Number	Description		Qty
SMPS PCB ASS'Y				
D921	HVDUF4007T	DIODE , SCHOTTKY	UF4007	1
D922	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)	1
D923	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)	1
D924	HVDSF26T	DIODE , SUPER FAST	SF26 (400V/2A)	1
IC91	BVISG6848DZ	IC,PWM	SG6848DZ	1
PC91	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1C	1
Q901	BVICEF04N6	FET , CEF04N6		1
Q903	HVTKSB1151Y	TRANSISTOR PNP	KSB1151Y	1
Resistors				
R901	KROS1TJ105V	RES , METAL FILM (1/2W , 1M OHM)	(1/2W , 1M OHM)	1
R903	CRD25TJ754T	RES	750K OHM 1/4W J	1
R904	CRD25TJ754T	RES	750K OHM 1/4W J	1
R905	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1
R906	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1
R907	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1
R909	CRD20TJ100T	RES , CARBON	10 OHM 1/5W J	1
R910	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1
R911	CRD20TJ104T	RES , CARBON	100K OHM 1/5W J	1
R912	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1
R913	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1
R914	CRD20TJ333T	RES , CARBON	33K OHM 1/5W J	1
R920	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1
R921	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1
R922	CRD20TF3481T	RES , CARBON	3.48K OHM 1/5W J	1
R923	CRD20TF3001T	RES , CARBON	3K 1/5W F	1
R924	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1
R925	CRD25TJ101T	RES , CARBON	100 OHM 1/4W J	1
R926	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1
R928	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1
R929	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1
R930	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1
R934	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1
R935	CRD20TJ153T	RES , CARBON	15K OHM 1/5W J	1
R940	CRD20TJ472T	RES , CARBON	4.7K OHM 1/5W J	1
R902	KRG1SANJ104H	RES,METAL OXIDE FILM	100K OHM	1
R908	KRW1PJ1R5V	RES, WIRE WOUND	1W 1.5(J) NON-I	1
R927	KRDS1TJ681V	RES , CARBON	680OHM 1/2W J	1
Miscellaneous				
	CVICEF04N6YA	FET. HEAT SINK ASS`Y	for Q901	1
CN91	KJP02KA060ZY	WAFER	7.92MM(YUNHO)	1
CN92	CJP12GA19ZY	WAFER	12Pin connector	1
	CMX1A176	INSULATOR, SMPS		1
FH91	KJCFC5S	HOLDER , FUSE		1
FH92	KJCFC5S	HOLDER , FUSE		1
L903	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5	1
L905	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5	1
NT91	KRT10D9MSFT	THERMISTER	10D9M	1
	CMY2A223	HEAT SINK		1
	CTB3+8J	SCREW		1
T901	CLT9Z018ZE	TRANSFORMER	EER2828H	1
LF91	CLZ9Z060Y	LINE FILTER	CLZ9Z060Y	1
F901	KBA2C2000TLEY	FUSE	EUR (2A/250V)	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
Capacitors				
C100	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C101	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C102	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C103	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C104	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C106	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C107	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C110	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C112	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C113	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C115	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C117	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C120	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C122	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C124	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C126	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C127	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C129	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C131	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C132	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C133	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C138	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C140	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C141	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C143	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C144	HCUS1H103KC	CAP , CHIP	0.01UF KC 1608	1
C146	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C148	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C149	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C151	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C152	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C153	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C154	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C156	HCUS1H180JA	CAP , CHIP	18PF JA 1608	1
C157	HCUS1H330JA	CAP , CHIP	33PF JA 1608	1
C158	HCUS1H330JA	CAP , CHIP	33PF JA 1608	1
C159	HCUS1H562KC	CAP , CHIP	5600PF KC 1608	1
C160	HCUS1H562KC	CAP , CHIP	5600PF KC 1608	1
C161	HCUS1H562KC	CAP , CHIP	5600PF KC 1608	1
C163	HCUS1H471JA	CAP , CHIP	470PF JA 1608	1
C164	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C165	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C166	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C167	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C168	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C169	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C170	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C172	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C173	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C174	HCUS1E333KC	CAP , CHIP	0.033PF KC 1608	1
C175	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C176	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C178	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C179	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C180	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
C181	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C183	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C185	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C186	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C187	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C188	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C189	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C190	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C191	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C192	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C193	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C194	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C195	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C196	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C197	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C199	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C200	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C201	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C204	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C205	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C207	HCUS1H272KC	CAP , CHIP	2700PF KC 1608	1
C208	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C209	HCUS1H273KC	CAP , CHIP	0.027UF KC 1608	1
C210	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C214	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C215	HCUS1H561JA	CAP , CHIP	560PF JA 1608	1
C217	HCUS1H273KC	CAP , CHIP	0.027UF KC 1608	1
C218	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C220	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C222	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C225	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C227	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C228	HCUS1H222KC	CAP , CHIP	2200PF KC 1608	1
C229	HCUS1H222KC	CAP , CHIP	2200PF KC 1608	1
C230	HCUS1H222KC	CAP , CHIP	2200PF KC 1608	1
C231	HCUS1H222KC	CAP , CHIP	2200PF KC 1608	1
C232	HCUS1H330JA	CAP , CHIP	33PF JA 1608	1
C234	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C235	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C237	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C240	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C242	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C244	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C245	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C247	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C249	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C250	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C252	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C253	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C254	HCUS1H272KC	CAP , CHIP	2700PF KC 1608	1
C255	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C256	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C257	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C260	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C261	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C262	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C263	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
C266	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C267	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C276	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C277	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C279	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C280	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C281	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C282	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C283	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C284	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C285	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C286	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C287	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C295	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C304	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V	1
C306	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V	1
C307	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V	1
C308	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V	1
C310	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C311	HCUS1H560JA	CAP , CHIP	56PF JA 1608	1
C312	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C313	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C336	HCUS1H682KB	CAP , CHIP	6800PF KB 1608	1
C337	HCUS1H223KC	CAP , CHIP	0.022UF KC 1608	1
C338	HCUS1H221JA	CAP , CHIP	220PF JA 1608	1
C339	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C346	HCUS1H7R0DT	CAP , CHIP	7PF D 1608	1
C380	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C401	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C402	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C403	HCUS1H102KC	CAP , CHIP	1000PF KC 1608	1
C405	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C406	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C408	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C429	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C430	CRJ10DJ0R0T	RES , CHIP	1608	1
C431	HCUS1H221JA	CAP , CHIP	220PF JA 1608	1
C432	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C511	HCUS1H151JA	CAP , CHIP	150PF JA 1608	1
C531	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C533	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C552	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C553	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C555	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C556	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C578	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C580	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C581	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C584	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C585	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C593	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C594	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C615	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C617	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C620	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C630	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C631	HCUS1H104ZF	CAP , CHIP	0.1UF ZF 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
C636	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C638	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C639	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C641	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C644	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C646	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C650	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C657	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C659	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C660	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C662	HCUS1H391JA	CAP , CHIP	390PF JA 1608	1
C664	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C665	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C668	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C671	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C672	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C674	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C677	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C678	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C679	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C809	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C810	HCUS1H560JA	CAP , CHIP	56PF JA 1608	1
C822	HCUS1H560JA	CAP , CHIP	56PF JA 1608	1
C823	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C828	HCUS1H220JA	CAP , CHIP	22PF JA 1608	1
C830	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C831	HCUS1H150JA	CAP , CHIP	15PF JA 1608	1
C834	HCUS1E104ZF	CAP , CHIP	0.1UF ZF 1608	1
C105	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C108	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C109	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C111	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C114	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C116	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C118	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C119	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C121	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C123	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C125	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C128	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C130	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C137	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C139	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C142	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C150	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C155	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C177	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C182	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C184	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C198	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C202	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C203	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C206	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C213	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C219	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C221	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C223	CCEA1CH101T	CAP , ELECT	100UF 16V	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
C224	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C226	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C233	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C236	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C241	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C243	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C251	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C258	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1
C301	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C404	CCEA1CKS470T	CAP , ELECT	47UF 16V	1
C504	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C508	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C510	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1
C530	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C532	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C548	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C549	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C561	CCEA1CH100T	CAP , ELECT	10UF 16V	1
C562	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1
C574	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C579	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C582	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C583	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C586	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C616	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C618	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C628	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C629	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C637	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C640	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C642	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C643	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C645	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C648	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C653	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C658	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C661	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C666	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C667	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C669	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C670	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C673	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C675	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C676	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1
C680	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C681	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C685	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C687	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C688	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C689	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C690	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C692	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J	1
C733	CCEA1HH3R3T	CAP , ELECT	3.3UF 50V	1
C751	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C752	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C795	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C801	CCEA1AH331T	CAP , ELECT	330UF 10V	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
C802	CCEA1AH331T	CAP , ELECT	330UF 10V	1
C803	CCEA1CH220T	CAP , ELECT	22UF 16V	1
C804	CCEA1CH101T	CAP , ELECT	100UF 16V	1
C824	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1
C825	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1
C826	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C827	CCEA1CH470T	CAP , ELECT	47UF 16V	1
C829	CCEA1AH471T	CAP , ELECT	470UF 10V	1
C835	CCEA1CH221T	CAP , ELECT	220UF 16V	1
C891	CCEA1AH471T	CAP , ELECT	470UF 10V	1
Semiconductors				
D101	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D102	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D501	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D502	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D511	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D601	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D602	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
D603	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1
IC10	HVIZR36778	IC,MPEG (ZORAN)	ZR36778	1
IC11	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1
IC12	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8	1
IC13	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1
IC14	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8	1
IC15	HVIAT24C08N10SC	I.C (EEPROM)	AT24C08N10SC2.7	1
IC16	HVISAA7893HLC2	IC,DSD DECODER (Philips)	SAA7893HL/C2 (P	1
IC17	HVI74VHC04MX	I.C , INVERTER	74VHC04M	1
IC18	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7T	1
IC19	HVIZR36721	IC,HDMI TRANSMITTER(ZORAN)	ZR36721	1
IC20	HVITL3472IDR	IC,OP AMP 8-SOIC (TI)	TL3472	1
IC21	HVIM29W160ET70N	IC,16M FLASH (ST)	M29W160ET-70N6	1
IC22	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7T	1
IC23	HVIAM5888SLF	I. C , Motor Driver(AMtek,Pb free)	AM5888S L/F	1
IC24	HVIZR36707	IC,RF (ZORAN)	ZR36707	1
IC40	HVICS4382-KQ	I.C , DAC	CS4382-KQ	1
IC41	BVIBH7862FS	IC , 6CH VIDEO DRIVER	ROHM (BH7862FS)	1
IC43	HVI74LVC157ADBR	I.C , MULTIPLEXER	SN74LVC157A	1
IC44	HVI74LVC157ADBR	I.C , MULTIPLEXER	SN74LVC157A	1
IC45	HVIST72F324K2	IC,FLASH (ST)	ST72F324K2	1
IC47	HVITC74HCT7007F	I.C	TC74HC7007AFEL	1
IC51	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117-1V8 (1.8V)	1
IC52	HVINJM2068MDTE1	I.C , OP AMP	NJM2068MD-TE1	1
IC53	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1
IC54	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1
IC55	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1
IC56	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117-5V0 (5V)	1
IC57	HVTHN1K05FU	MOS FET	HN1K05FU	1
Q105	HVTKTA1664YP	TRANSISTOR PNP	KTA1664	1
Q106	HVTKTA1664YP	TRANSISTOR PNP	KTA1664	1
Q108	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1
Q109	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1
Q110	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1
Q307	HVT2SA1955B	TRANSISTOR, TE85L,F, SSM Type	TE85L,F SSM TYP	1
Q308	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1
Q315	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
Q404	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1
Q407	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1
Q408	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q501	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1
Q502	HVTKTC3875SYRTK	TRANSISTOR , CHIP	KTC3875S Y RTK	1
Q604	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q606	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q607	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q608	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1
Q609	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q610	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q611	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q612	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q613	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q614	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q615	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q616	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1
Q617	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q618	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q619	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q620	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q621	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q622	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q804	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1
Q805	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1
Q806	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1
Q821	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1
IC50	HVIKA79L08AZT	REGULATOR, -8V	KA79L08	1
Q605	HVTKSA916YT	TRANSISTOR PNP	KSA916Y	1
D103	KVD1N4003ST	DIODE	1N4003	1
D104	KVD1N4003ST	DIODE	1N4003	1
D105	KVD1N4003ST	DIODE	1N4003	1
D107	KVD1N4003ST	DIODE	1N4003	1
D109	KVD1N4003ST	DIODE	1N4003	1
D110	KVD1N4003ST	DIODE	1N4003	1
D401	CVD50BOBBWGA	L.E.D , 2 COLOR (ORG , BLUE)	TOL-50BOBBWGA	1
IC46	BVIKP1010B	IC, PHOTO COUPLER	KP1010	1
IC49	HVIKIA7808API	REGULATOR, +8V	KIA7808 (KEC)	1
IC61	HRVKSM603TH2	SENSOR IR	KSM-603TH2	1
Resistors				
R100	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R101	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608	1
R102	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R103	CRJ10DF4300T	RES	430 OHM(1%) 1608	1
R104	CRJ10DF3920T	RES. CHIP (392R 1%)	392 OHM(1%)1608	1
R105	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R106	CRJ104DJ101T	RES, ARRAY, 100R (1608)	100R (1608)	1
R107	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R108	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R109	CRJ10DJ472T	RES , CHIP	100 OHM 1608	1
R110	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R111	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R112	CRJ10DJ202T	RES , CHIP	2K OHM 1608	1
R113	CRJ10DJ202T	RES , CHIP	2K OHM 1608	1
R114	CRJ10DJ121T	RES , CHIP	120 OHM 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R115	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R116	CRJ10DJ121T	RES , CHIP	120 OHM 1608	1
R117	CRJ10DJ121T	RES , CHIP	120 OHM 1608	1
R118	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R119	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R120	CRJ10DJ123T	RES , CHIP	12K OHM 1608	1
R121	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R122	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R123	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R124	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R125	CRJ10DJ113T	RES , CHIP	11K OHM 1608	1
R126	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R127	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R128	CRJ10DJ121T	RES , CHIP	120 OHM 1608	1
R129	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R130	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R131	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R132	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R133	CRJ10DF3920T	RES. CHIP (392R 1%)	392 OHM(1%) 1608	1
R134	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R135	CRJ10DJ100T	RES , CHIP	10 OHM 1608	1
R136	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R137	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R138	CRJ10DJ100T	RES , CHIP	10 OHM 1608	1
R139	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R140	CRJ10DJ133T	RES , CHIP	13K OHM 1608	1
R141	CRJ10DJ474T	RES , CHIP	470K OHM 1608	1
R142	CRJ10DJ474T	RES , CHIP	470K OHM 1608	1
R143	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R144	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R145	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R146	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R147	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R148	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R149	CRJ104DJ470T	RES , 4ARRAY (1608*4)	47 OHM/1608X4	1
R150	CRJ104DJ470T	RES , 4ARRAY (1608*4)	47 OHM/1608X4	1
R151	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R152	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R153	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R154	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R155	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R156	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R157	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R158	CRJ104DJ101T	RES, ARRAY, 100R (1608)	100 OHM/1608X4	1
R159	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R160	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R161	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R162	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R163	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R164	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R165	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R166	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R167	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R168	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R169	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R170	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R171	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R172	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R173	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R174	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R175	CRJ10DJ912T	RES , CHIP	9.1K OHM/1608	1
R176	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R177	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R178	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608	1
R180	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R181	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R182	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R183	CRJ10DF1202T	RES , CHIP 1%	1.2K OHM(1%) 1608	1
R184	CRJ10DJ471T	RES , CHIP	470 OHM 1608	1
R185	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R186	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R187	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R188	CRJ10DJ113T	RES , CHIP	11K OHM 1608	1
R189	CRJ10DJ105T	RES , CHIP	1M OHM 1608	1
R190	CRJ10DJ223T	RES , CHIP	22K OHM 1608	1
R191	CRJ10DJ223T	RES , CHIP	22K OHM 1608	1
R192	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R193	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R194	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R195	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R196	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R197	CRJ10DJ753T	RES , CHIP	75K OHM 1608	1
R198	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R199	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R200	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R201	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R202	CRJ10DJ622T	RES , CHIP	6.2K OHM 1608	1
R203	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R204	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R205	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R206	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R207	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608	1
R209	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608	1
R210	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608	1
R211	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608	1
R212	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R213	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R214	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R215	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R216	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R217	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R218	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1
R219	CRJ10DJ273T	RES , CHIP	27K OHM 1608	1
R220	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R221	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R222	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608	1
R223	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R224	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R225	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R226	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R227	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R228	CRJ10DJ330T	RES , CHIP	33 OHM 1608	1
R230	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R241	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM(1%) 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R243	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM(1%) 1608	1
R244	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1% 1608	1
R265	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R284	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R285	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R287	CRJ10DJ113T	RES , CHIP	11K OHM 1608	1
R297	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R298	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R299	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R301	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R302	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R303	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R305	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R306	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R307	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608	1
R308	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R309	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R377	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R404	CRJ10DJ333T	RES , CHIP	33K OHM 1608	1
R409	CRJ10DJ100T	RES , CHIP	10 OHM 1608	1
R410	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R412	CRJ10DJ681T	RES , CHIP	680 OHM 1608	1
R413	CRJ10DJ821T	RES , CHIP	820 OHM 1608	1
R414	CRJ10DJ122T	RES , CHIP	1.2K OHM 1608	1
R415	CRJ10DJ152T	RES , CHIP	1.5K OHM 1608	1
R416	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R417	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R418	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1
R419	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R420	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R421	CRJ10DJ680T	RES , CHIP	68 OHM 1608	1
R422	CRJ10DJ121T	RES , CHIP	120 OHM 1608	1
R423	CRJ10DJ820T	RES , CHIP	82 OHM 1608	1
R424	CRJ10DJ4R7T	RES , CHIP	4.7 OHM 1608	1
R425	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R501	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608	1
R502	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608	1
R503	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R504	CRJ10DJ473T	RES , CHIP	47K OHM 1608	1
R505	CRJ10DJ470T	RES , CHIP	47 OHM 1608	1
R506	CRJ10DJ271T	RES , CHIP	270 OHM 1608	1
R511	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R512	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R513	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R514	CRJ10DJ100T	RES , CHIP	10 OHM 1608	1
R515	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R516	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R517	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R518	CRJ10DJ103T	RES , CHIP	10K OHM 1608	1
R519	CRJ10DJ473T	RES , CHIP	47K OHM 1608	1
R522	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R533	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R544	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R549	CRJ10DJ105T	RES , CHIP	1M OHM 1608	1
R552	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R553	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R564	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R593	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R600	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R601	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R602	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R603	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R604	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R605	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R606	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R607	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R608	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R609	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R611	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R612	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R618	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R619	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R620	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R621	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R622	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R623	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R624	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R625	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R626	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R627	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R628	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R629	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R630	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R631	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R632	CRJ10DJ104T	RES , CHIP	1M OHM 1608	1
R633	CRJ10DJ104T	RES , CHIP	1M OHM 1608	1
R641	CRJ10DJ224T	RES , CHIP	220K OHM 1608	1
R642	CRJ10DJ224T	RES , CHIP	220K OHM 1608	1
R650	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R651	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R652	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R653	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R654	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R655	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R656	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R657	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R658	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R659	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R660	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R661	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R662	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R663	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R664	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R665	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R666	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R667	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R668	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R669	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R670	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R671	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R672	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R673	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R674	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608	1
R675	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1

Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R676	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R677	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R678	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R679	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R680	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R681	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R682	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R683	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R684	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R685	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R686	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R687	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R688	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R689	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R690	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R691	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R692	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R694	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R695	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R698	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R699	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608	1
R726	CRJ10DJ474T	RES , CHIP	470K OHM 1608	1
R727	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R728	CRJ10DJ223T	RES , CHIP	22K OHM 1608	1
R729	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R730	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R731	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R732	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R733	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R734	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R735	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R736	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R737	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R738	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R739	CRJ10DJ224T	RES , CHIP	220K OHM 1608	1
R744	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R745	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R746	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R747	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R748	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R749	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R801	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R802	CRJ10DJ820T	RES , CHIP	82 OHM 1608	1
R803	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R806	CRJ10DJ820T	RES , CHIP	82 OHM 1608	1
R816	CRJ10DJ390T	RES , CHIP	39 OHM 1608	1
R817	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R818	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R821	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R823	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608	1
R824	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R825	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R826	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608	1
R827	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R828	CRJ18AJ221T	RES , CHIP	220 OHM 1608	1
R829	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R830	CRJ10DJ390T	RES , CHIP	39 OHM 1608	1

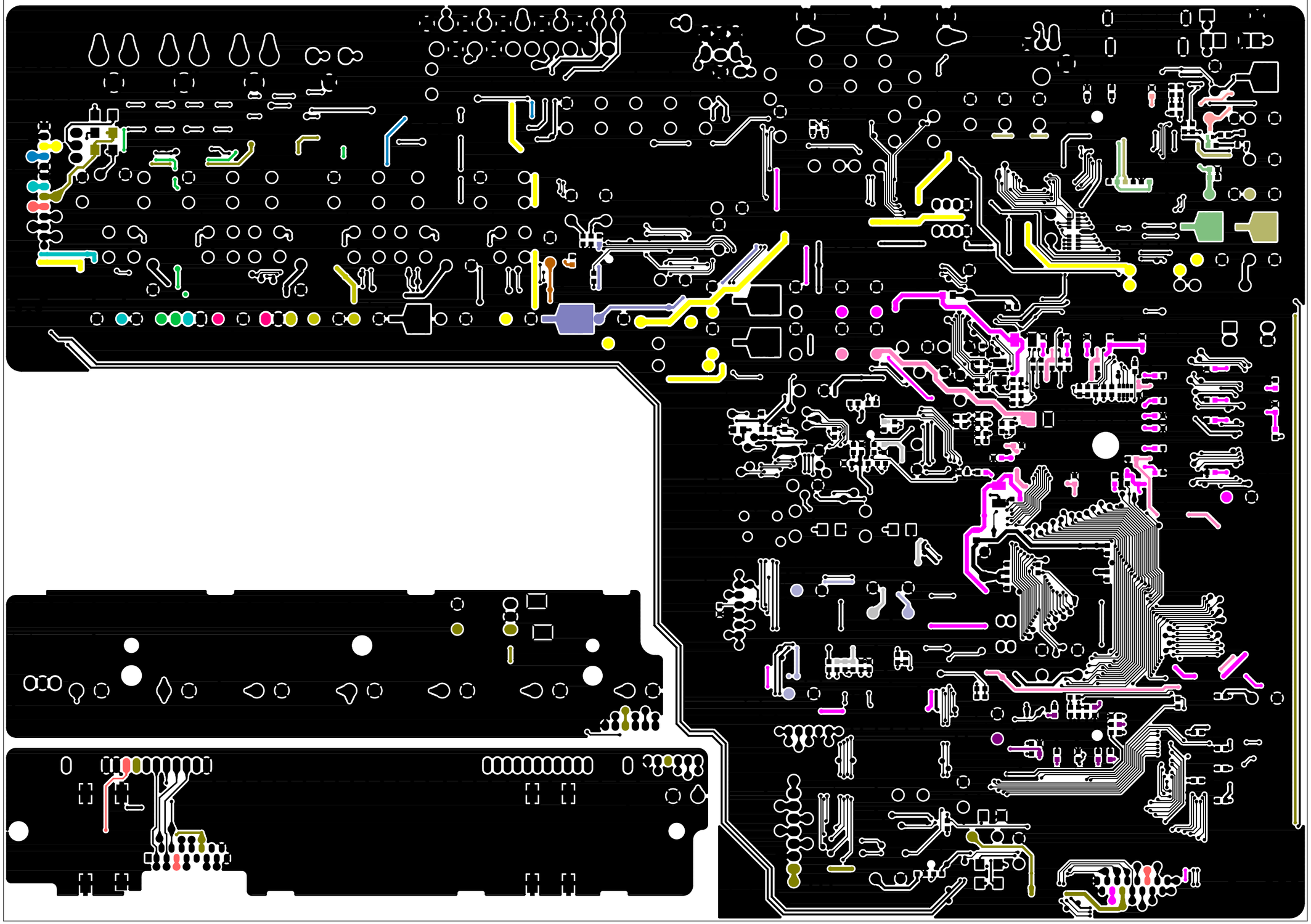
Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
R832	CRJ10DJ102T	RES , CHIP	1K OHM 1608	1
R833	CRJ10DJ750T	RES , CHIP	75 OHM 1608	1
R834	CRJ10DJ820T	RES , CHIP	82 OHM 1608	1
R878	CRJ10DJ104T	RES , CHIP	100K OHM 1608	1
R879	CRJ10DJ101T	RES , CHIP	100 OHM 1608	1
R895	CRJ10DJ221T	RES , CHIP	220 OHM 1608	1
R896	CRJ10DJ680T	RES , CHIP	68 OHM 1608	1
Miscellaneous				
CN11	KJP24GA195ZM	SMT FFC/FPC WAFER(0.5MM PITCH)	52559-2472 (PB	1
X101	HOX27000E180S	CRYSTAL , CHIP(27MHZ,SMD)	27MHz, HC-49/US	1
JK07	HJJ9H003Z	JACK,HDMI (JALCO)	YKF45-7009	1
L101	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L102	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L103	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L104	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L105	HLQ06E100KRZ	INDUCTOR , CHIP	3225	1
L106	HLQ06E100KRZ	INDUCTOR , CHIP	3225	1
L107	HLQ06E100KRZ	INDUCTOR , CHIP	3225	1
L109	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L110	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L111	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L112	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L113	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L114	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L115	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L116	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L117	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L118	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L119	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L120	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L121	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L122	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L123	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L124	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L125	HLZ9R006Z	BEAD , CHIP	221E, 1.5A	1
L126	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L127	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L128	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L217	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L518	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L519	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L520	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L521	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L522	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L601	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900	1
L602	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900	1
L603	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900	1
L604	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900	1
L610	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L611	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L612	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L613	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L614	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L615	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L616	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1

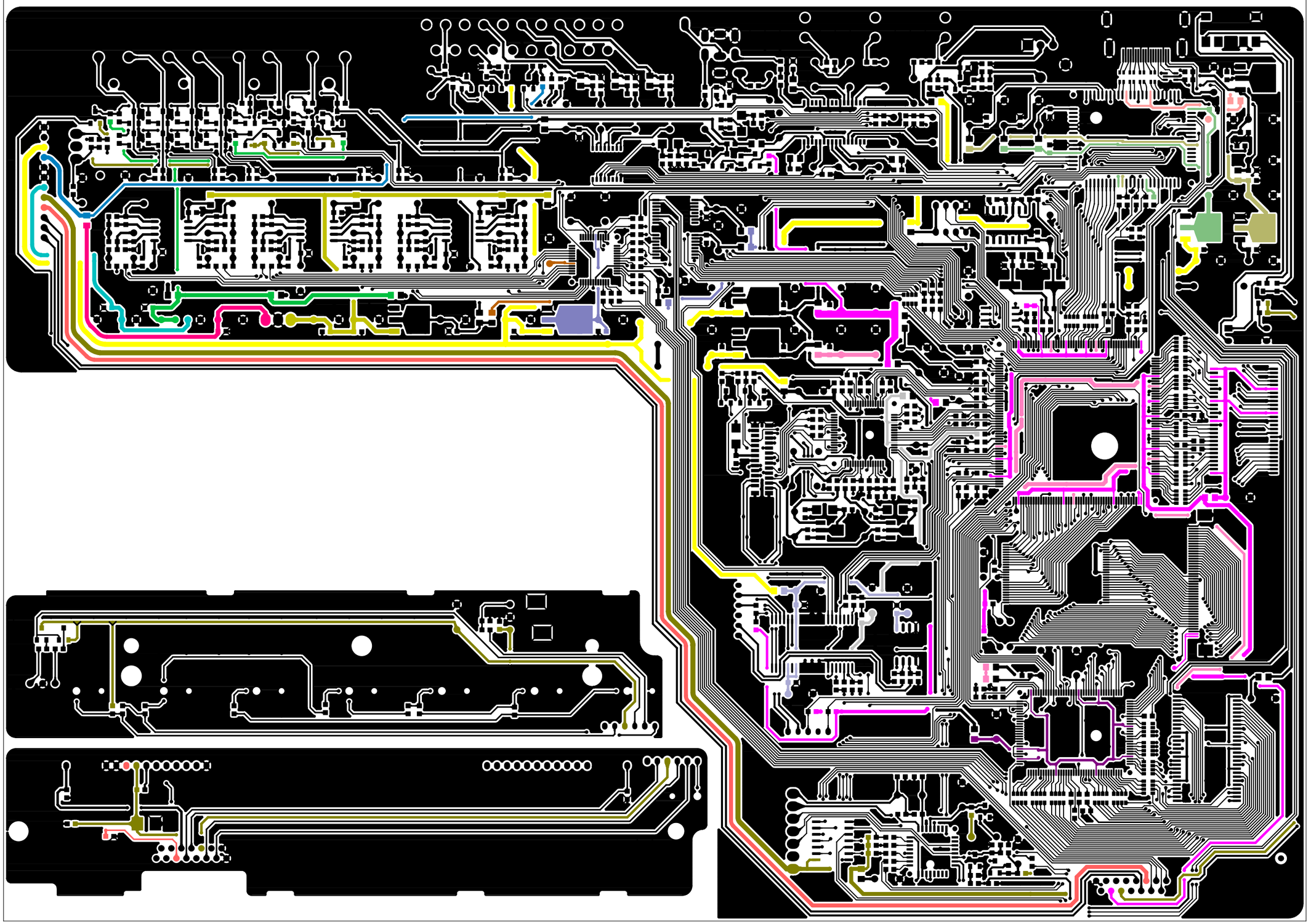
Ref. Designator	Part Number	Description		Qty
MAIN/FRONT PCB ASS'YS				
L617	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L696	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L801	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1
L804	HLQ09E8R2KRZ	CHIP , COIL	8.2UH 2012	1
L805	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1
L806	HLQ08ER39KRZ	CHIP FERRITE INDUCTOR	2012-R39UH	1
L808	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1
L809	HLQ09E8R2KRZ	CHIP , COIL	8.2UH	1
S401	HST1A020ZT	SW , TACT	switch, Front panel	1
S402	HST1A020ZT	SW , TACT	switch, Front panel	1
S403	HST1A020ZT	SW , TACT	switch, Front panel	1
S404	HST1A020ZT	SW , TACT	switch, Front panel	1
S405	HST1A020ZT	SW , TACT	switch, Front panel	1
S406	HST1A020ZT	SW , TACT	switch, Front panel	1
S407	HST1A020ZT	SW , TACT	switch, Front panel	1
S408	HST1A020ZT	SW , TACT	switch, Front panel	1
	CMD1A504	BRACKET , FIP		2
BN01	CWB1C912060EN	WIRE ASS'Y	12Pin, 60mm	1
BN07	CWB1A906190EN	WIRE ASS'Y	6Pin, 190mm	1
CN01	CJP15GA117ZY	WAFER , CARD CABLE	15Pin connector	1
CN03	CJP07GA01ZY	WAFER, STRAIGHT, 7PIN	7Pin connector	1
CN05	CJP15GB113ZY	WAFER	15Pin connector	1
CN07	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector	1
CN12	CJP05GA19ZY	WAFER, STRAIGHT, 5PIN	5Pin connector	1
CN13	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector	1
ET01	CMC1A111	PLATE , EARTH		1
ET02	CMC1A111	PLATE , EARTH		1
F401	HFL13BT229GINK	F.I.P (Fluorescent Indicator Panel)	13-BT-229GINK (	1
JK01	CJJ4R041Z	6P JACK, BOARD	RCA-601DAG-11	1
JK02	CJJ4N067Z	2P, JACK	RCA-201DAG-01	1
JK03	CJJ4S043Z	JACK , BOARD		1
JK04	CJJ9N003Z	JACK , (S-VIDEO+VHS)		1
JK06	HJS9U008Z	Optical+Coaxial Jack (Gold Plate)	YKC22-0732N	1
JK08	HJJ1D002Z	JACK, HOSIDEN	SR7400	1
X501	HOX08000E160C	CRYSTAL 8MHz		1
	CTB3+10G	SCREW		2
	CTB3+6FFZ	SCREW		1
	CTB3+8G	SCREW		3
	CTW3+8J	SCREW		7
	CUA2A259	CHASSIS, BOTTOM		1
	CWZDVD37BN91A	IN-LET WIRE ASS'Y	DVD37/47	1
	CJJ8A004Z	RECEPTACLE,(2.5A 250V AC) UL		1
	CWZDVD37BN91	WIRE ASS'Y	UL1617 AWG#18	1
	KHG1A050	RUBBER , CUSHION		4
	KHG1A326Z	LUG CUSHION		2
	KMC1A264	cushion,shield		1
Miscellaneous/Mechanical				
	CARTDVD47	REMOCON ASS'Y		1
	CHE154	CLAMPER , ARM		0.12
	CGWDVD47	FRONT PANEL ASS'Y		1
	CBT1A997	KNOB, FUNCTION		1
	CGL1A240	INDICATOR, POWER		1
	CGR1A387K128	DOOR, DVD		1
	CGUDVD47ZA	WINDOW ASS'Y		1

Ref. Designator	Part Number	Description		Qty
Miscellaneous/Mechanical				
	CGU1A383Z	WINDOW, FIP		1
	KGB1A164Z	BADGE, DVD47		1
	CGW2A413RDH43	PANEL,FRONT		1
	CGX1A374YC23	ORNAMENT, DOOR		1
	CMZ1A105Z	FILTER, FIP		1
	CTB3+10G	SCREW		5
	CTB3+6J	SCREW		2
	CWC1B2A15A120B	CABLE , CARD		1
	KGB1A158Z	BADGE , HARMAN/KARDON(FRONT)		1
	CGX1A375ZA	BADGE ASS'Y		1
	CGX1A375M7G32	ORNAMENT , BADGE		1
	KGB1A159Z	BADGE , HARMAN/KARDON(TOP)		1
	CKC2B166S46	CABINET, TOP		1
	CTBD3+10GFZ	SCREW , DOT		6
	CTBD3+8JFC	SCREW , DOT		4
	CUADVD47	BOTTOM CHASSIS ASS'Y		1
	CHR301	CLAMPER		2
	CJDDVD27YA	MECHANISM ASS'Y		1
	CADSDL003YA	LOADER ASS'Y		1
	CMH1A250	GUIDE, CABLE		1
	CWB1B905150EE	WIRE ASS'Y		1
	CWB5A906150SE	WIRE ASS'Y		1
	CWC1G2A24G250B	CABLE , CARD		1
	CKF3A303Z	PANEL, REAR		1
	CKL2A186H43	FOOT		4

< A30C5/C5 >

< A30C5/C5 >





CIRRUS LOGIC®

CS4382

114 dB, 192 kHz 8-Channel D/A Converter

Features

- 24-Bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM and DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Dedicated DSD inputs
- Low Clock Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- µC or Stand-Alone Operation

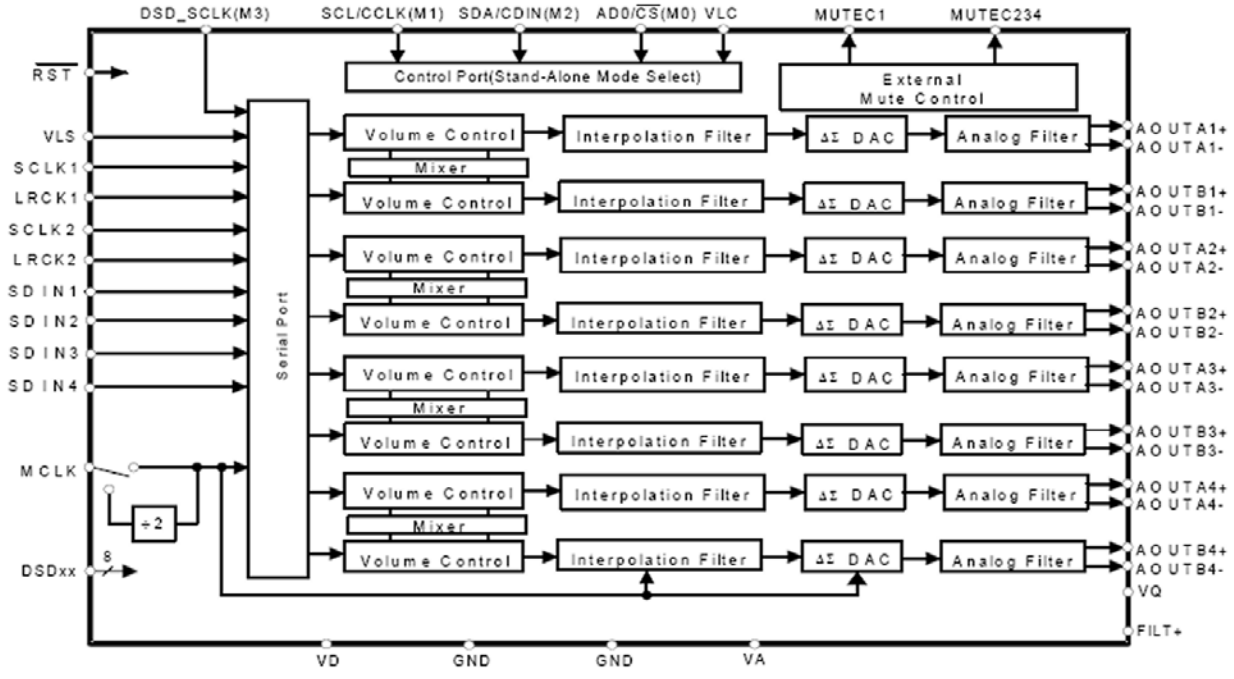
Description

The CS4382 is a complete 8-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4382 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players, SACD players, A/V receivers, digital TV's and VCR's, mixing consoles, effects processors, set-top boxes, and automotive audio systems.

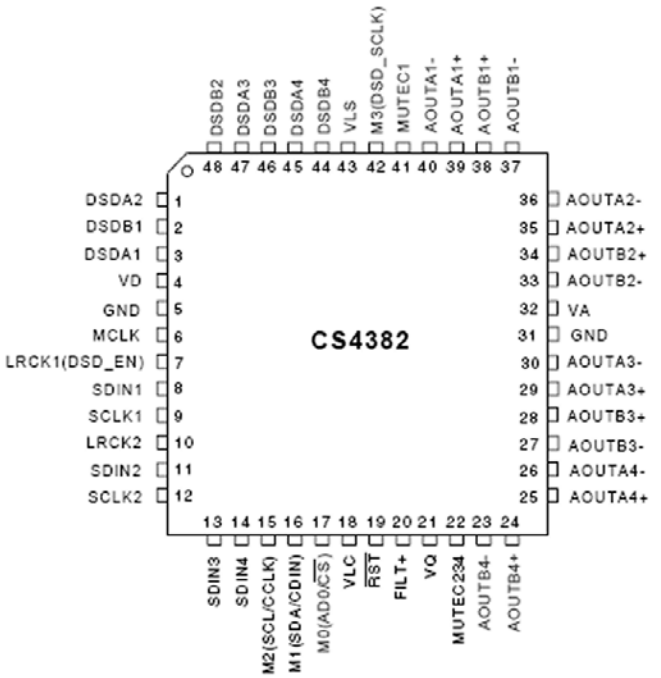
ORDERING INFORMATION

CS4382-KQZ, Lead Free	-10 to 70 °C	48-pin LQFP
CS4382-BQ	-40 to 85 °C	48-pin LQFP
CDB4382		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

4. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequency.
LRCK1 LRCK2	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 SCLK2	9 12	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.

Pin Name	#	Pin Description
MUTEC1 **MUTEC234**	41 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. These pins are intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	39, 40 38, 37 35, 36 34, 33 29, 30 28, 27 25, 26 24, 23	**Differential Analog Output** (*Output*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
Control Port Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	17	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Definitions		
M0 **M1** **M2** **M3**	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 6 and 7.
DSD Definitions		
DSD_SCLK	42	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface.
DSD_EN	7	**DSD-Enable** *(Input)* - When held at logic '1' the device will enter DSD mode (Stand-Alone mode only).
DSDA1 **DSDB1** **DSDA2** **DSDB2** **DSDA3** **DSDB3** **DSDA4** **DSDB4**	3 2 1 48 47 46 45 44	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data.

ESMT **M12L64164A**

SDRAM 1M x 16 Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

ORDERING INFORMATION

54 Pin TSOP (Type II)
(400mil x 875mil)

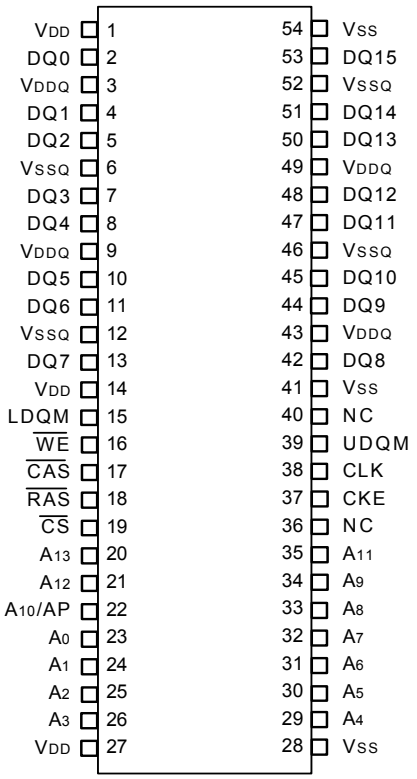
PRODUCT NO.	MAX FREQ.	PACKAGE
M12L64164A-6T	166MHz	TSOP II
M12L64164A-7T	143MHz	

GENERAL DESCRIPTION

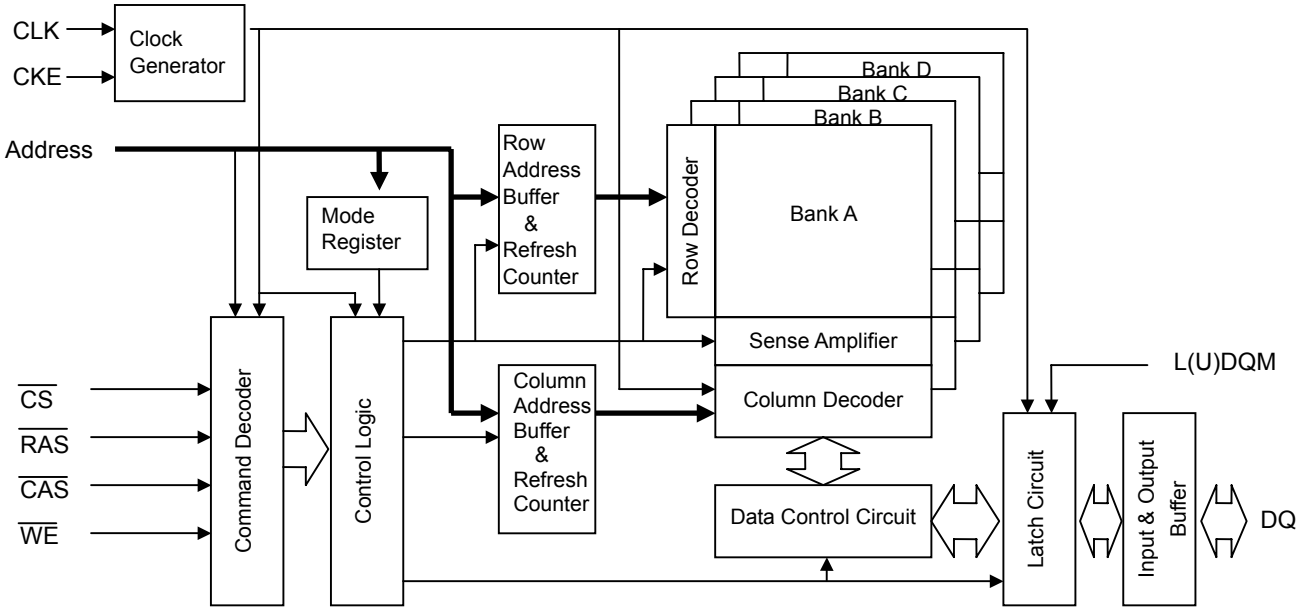
The M12L64164A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

PIN ASSIGNMENT

Top View



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (A13~A12)

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A13~A12 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed A13~A12 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A11)

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with $\overline{RAS}$ and A13~A12 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and A13~A12 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and A13~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and A13~A12. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and A13~A12 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SDRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $t_{RAS\ (max)}$ and $t_{RAS\ (max)}$ can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid A13~A12 of the bank to be procharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS\ (max)}$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RFC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or the burst of 4096 auto refresh cycles in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

TOSHIBA TC74HCT7007AP/AF

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

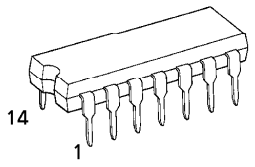
TC74HCT7007AP, TC74HCT7007AF

HEX BUFFER

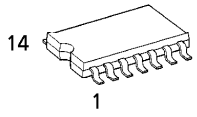
The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 11ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 1μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IH} = 2V (Min.)
  V_{IL} = 0.8V (Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS07

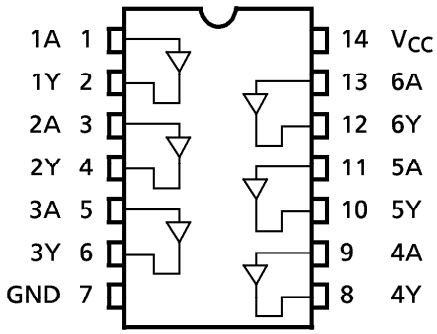


P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



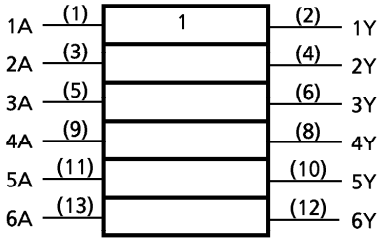
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



PIN ASSIGNMENT

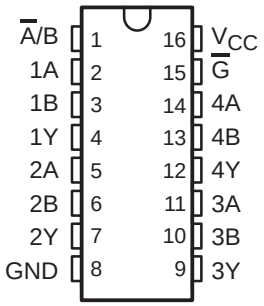
A	Y
L	L
H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC157A features a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC157A is characterized for operation from –40°C to 85°C.

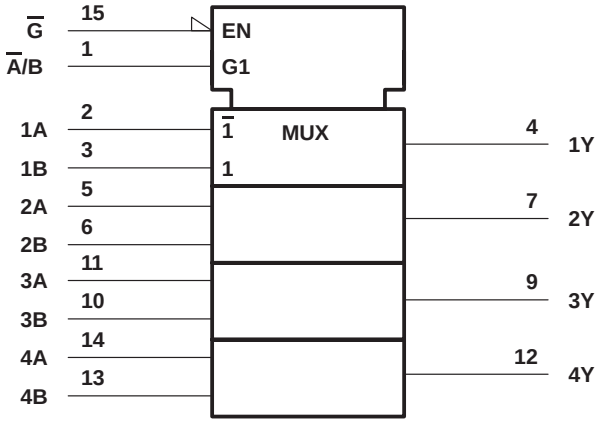
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

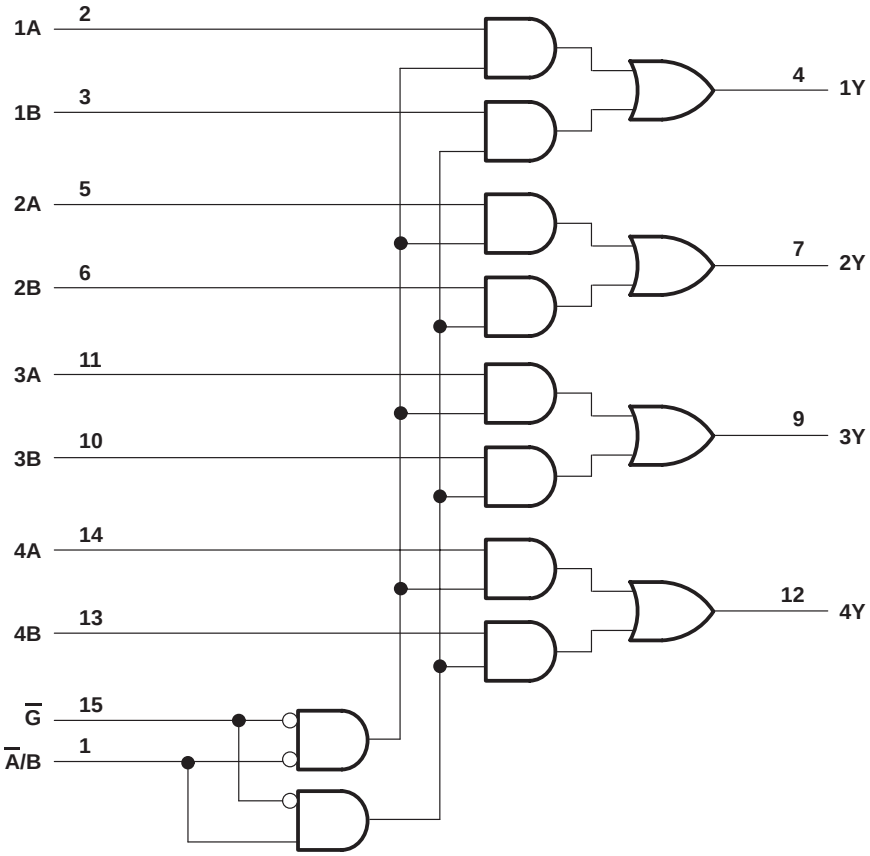
SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FAIRCHILD SEMICONDUCTOR®

November 1992
Revised February 2005

74VHC04
Hex Inverter

General Description

The VHC04 is an advanced high speed CMOS Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 3.8 ns (typ) at V_{CC} = 5V
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power down protection is provided on all inputs
- Low Noise: V_{OLP} = 0.4V (typ)
- Low power dissipation: I_{CC} = 2 μA (Max) @ T_A = 25°C
- Pin and function compatible with 74HC04

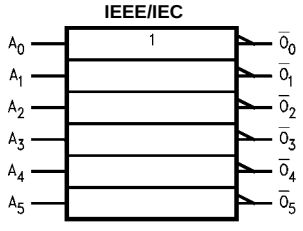
Ordering Code:

Order Number	Package Number	Package Description
74VHC04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC04MX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC04SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC04MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

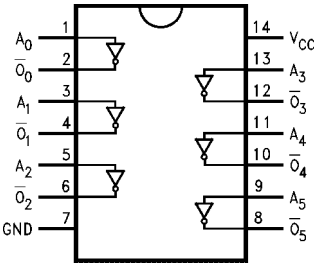
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	$\overline{O}$
L	H
H	L

5-channel BTL Driver for DVD player AM5888S

The AM5888S is a five-channel BTL driver IC for driving the motors and actuators such as used in DVD player and consists of two independent precision voltage regulators with adjustable range from 1.5V to 4 V. It supports a variety of applications. Also, Pb free package is selectable (Please refer to Marking Identification).

● Applications

BTL driver for CD, CD-ROM and DVD.

● Features

1) Two channels are voltage-type BTL drivers for actuators of tracking and focus. Two channels are voltage-type BTL driver for sled and spindle motors. It is also built-in one channel bi-direction DC motor driver for tray.
2) Wide dynamic range [9.0V (*typ.*) when Vcc1= Vcc2= 12V, at R_L= 20Ω load].
3) Separating power of Vcc1 and Vcc2 is to improve power efficiency by a low supply voltage for tracking, focus, and spindle.
4) Level shift circuit built-in.
5) Thermal shut down circuit built-in.
6) Mute mode built-in.
7) **Dual actuator drivers:**
   A general purpose input OP provides differential input for signal addition. The output structure is two power OPAMPS in bridge configuration.
8) **Sled motor driver:**
   A general purpose input OP provides differential input for signal addition. The output structure is one power OPAMP in bridge configuration.
9) **Spindle driver:**
   Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.
10) **Tray in-out driver:**
    The DC motor driver supports forward/reverse control for tray motor.
11) 2 **Built-in regulator controllers**
    Adjustable range 1.5V ~ 4V

● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc1 Vcc2	13.5	V
Power dissipation	P_d	*1.7	W
Operate Temp range	T_{opr}	-35 ~ +85	℃
Storage Temp range	T_{stg}	**-55 ~ +150	℃

*When mounted on a 70mm×70mm×1.6mm glass epoxy board.

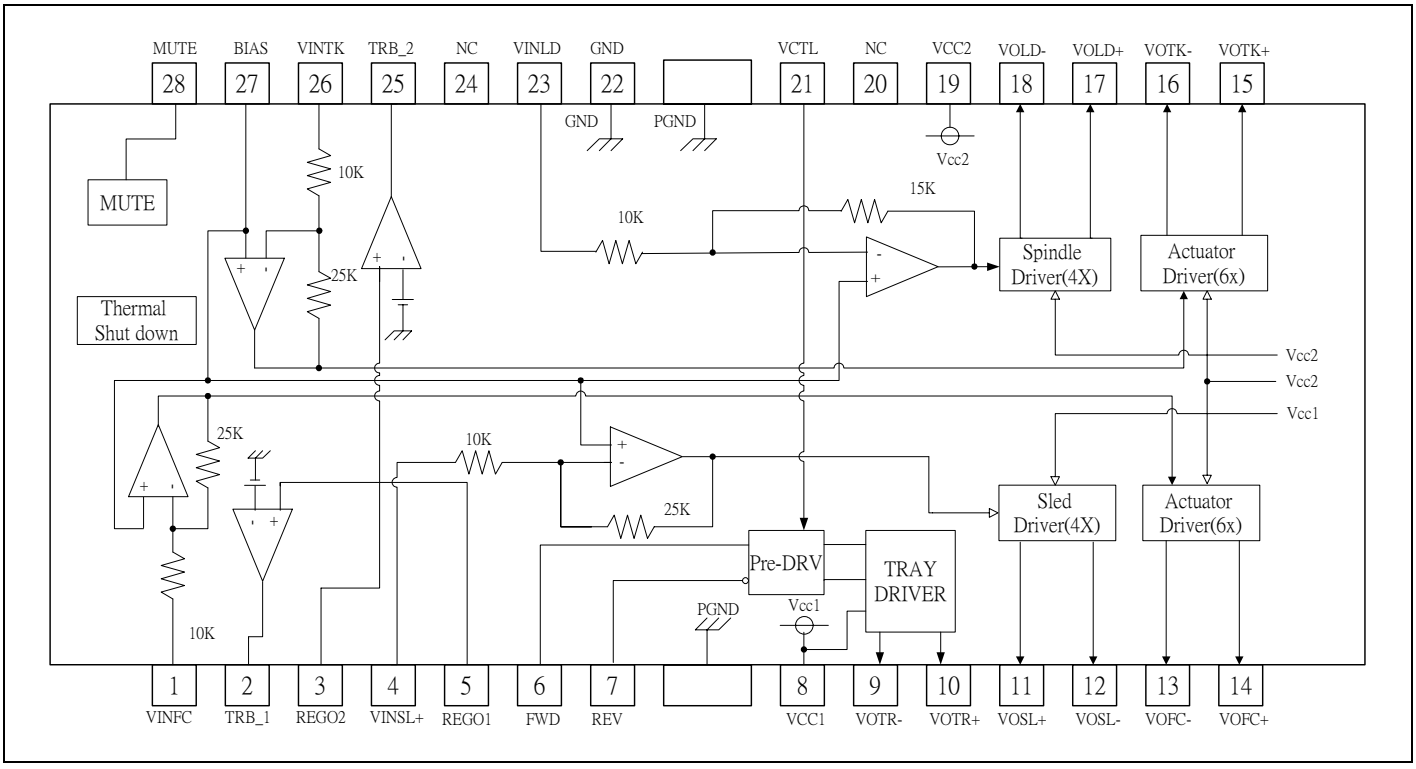
*Reduced by 13.6mW for each increase in T_a of 1℃ over 25℃.

**Should not exceed Pd or ASO and T_j=150℃ values

● Guaranteed operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc1	4.3 ~ 13.2	V
	Vcc2	4.3 ~ Vcc1	V

● Block diagram



● Pin description

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	Connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output (-)
10	VOTR+	Tray driver output (+)
11	VOSL+	Sled driver output (+)
12	VOSL-	Sled driver output (-)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Spindle driver output (+)
18	VOLD-	Spindle driver output (-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	NC	No Connection
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	NC	No Connection
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

Notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example, if voltage of pin1 is high, pin14 is high.)

Features

- **Medium-voltage and Standard-voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Automotive Temperature Range –40°C to 125°C**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz (2.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages**

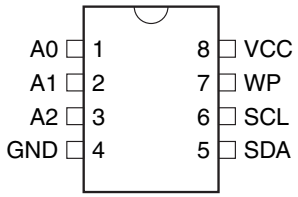
Description

The AT24C01A/02/04/08A/16A provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08A/16A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages and is accessed via a two-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) versions.

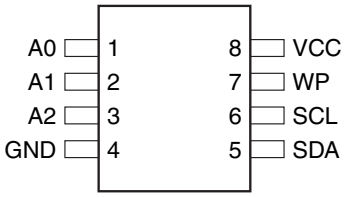
Table 1. Pin Configurations

Pin Name	Function
A0 – A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

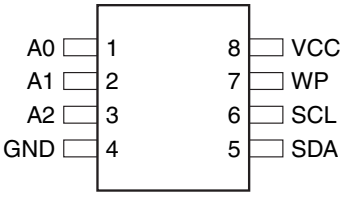
8-lead PDIP



8-lead SOIC



8-lead TSSOP



Two-wire Automotive Temperature Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08A
AT24C16A

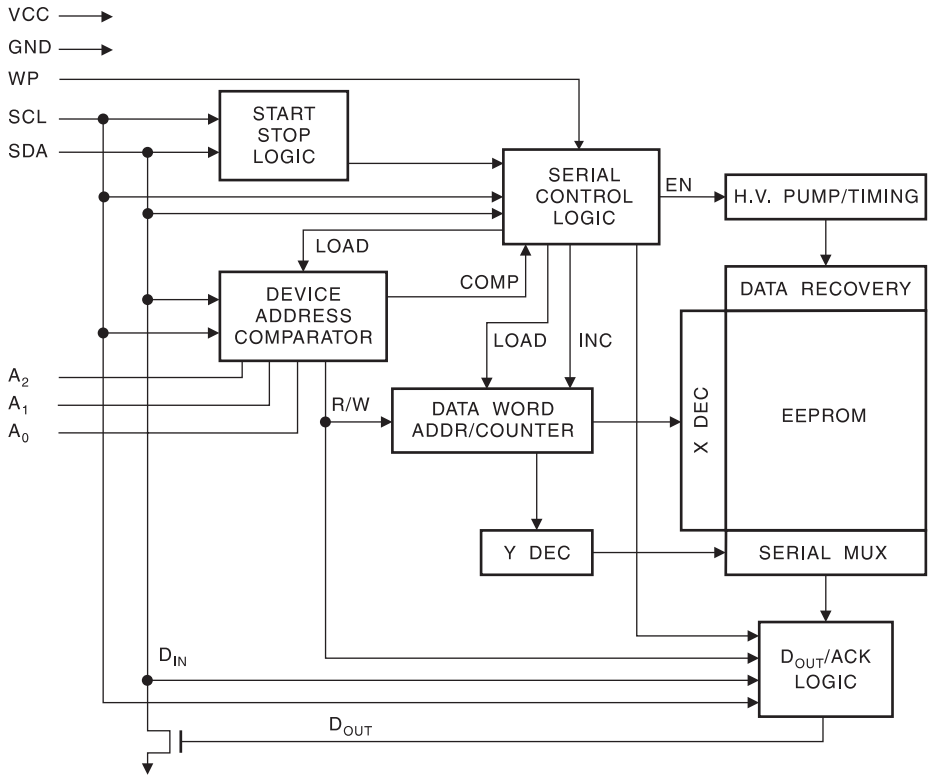
5092B–SEEPR–9/05

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

AT24C01A/02/04/08A/16A

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16A does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/08A/16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 2. Write Protect

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08A	24C16A
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Full (8K) Array	Full (16K) Array
At GND	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08A, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16A, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

AT24C01A/02/04/08A/16A

Table 5. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to +125°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	AT24C01A/02/04/08A/16A		Units
		Min	Max	
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(2)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(2)		300	ns
t_F	Inputs Fall Time(2)		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(2)	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. This parameter is characterized.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 5 on page 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 on page 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08A/16A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

3-channel 75Ω driver

BA7660FS

Multimedia ICs

The BA7660FS is a 75Ω driver with a 6dB amplifier and three internal circuits, and provides 75Ω drive of composite Y signals and C signals, as well as RGB signals. Each load is capable of driving two circuits, and a sag correction function reduces the capacitance of the output coupling capacitor.
The input voltage is within a range of 0V to 1.5V, enabling direct connection of ordinary D / A converter output. An internal power-saving circuit is also included which provides simultaneous muting on all three channels, and output pin shorting protection.

●Applications
DVDs, set top boxes and other digital video devices

●Features
1) Can be coupled directly to D / A converter output.
2) Operates at a low power consumption (115mW typ.).
3) Internal output muting circuit.
4) Internal power-saving circuit.
5) Internal output protection circuit.
6) An internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
7) Each load is capable of driving two circuits.
8) The compact 16-pin SSOP-A package is used.

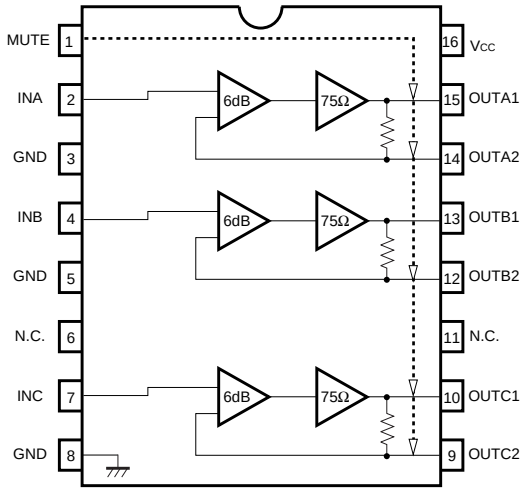
●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8	V
Power dissipation	Pd	650	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	Vcc	4.5	5.0	5.5	V

●Block diagram



MUTE (1pin)

H	3ch MUTE
L	NORMAL

BH7862FS

Multimedia ICs

High-performance 6-channel video driver IC for progressive DVD

BH7862FS

BH7862FS is a 6-channel video driver IC developed for progressive DVD player/recorder. Special filters adjusted to each band of various video signals are incorporated into a single chip. Extended definition, size reduction, and high cost performance can be achieved in DVD players.

●Application

DVD players, DVD recorders

●Features

1) Each high-performance filter, 6dB amplifier, and 75Ω driver for DVD are incorporated into a single chip.
2) Driver 6ch (Y, C, MIX, and PY, Pb, Pr for progressive)
3) Group delay difference between chroma signal and luminance signal is a small number of nsec.
4) Drive 2 lines of each signal
5) Operating by 5V single power supply
6) Built-in mute circuit

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Impressed voltage	V_{CC} max	6.0	V
Power dissipation	Pd	0.95*	W
Operating temperature range	Topr	−10~+70	°C
Storage temperature range	Tstg	−55~+150	°C

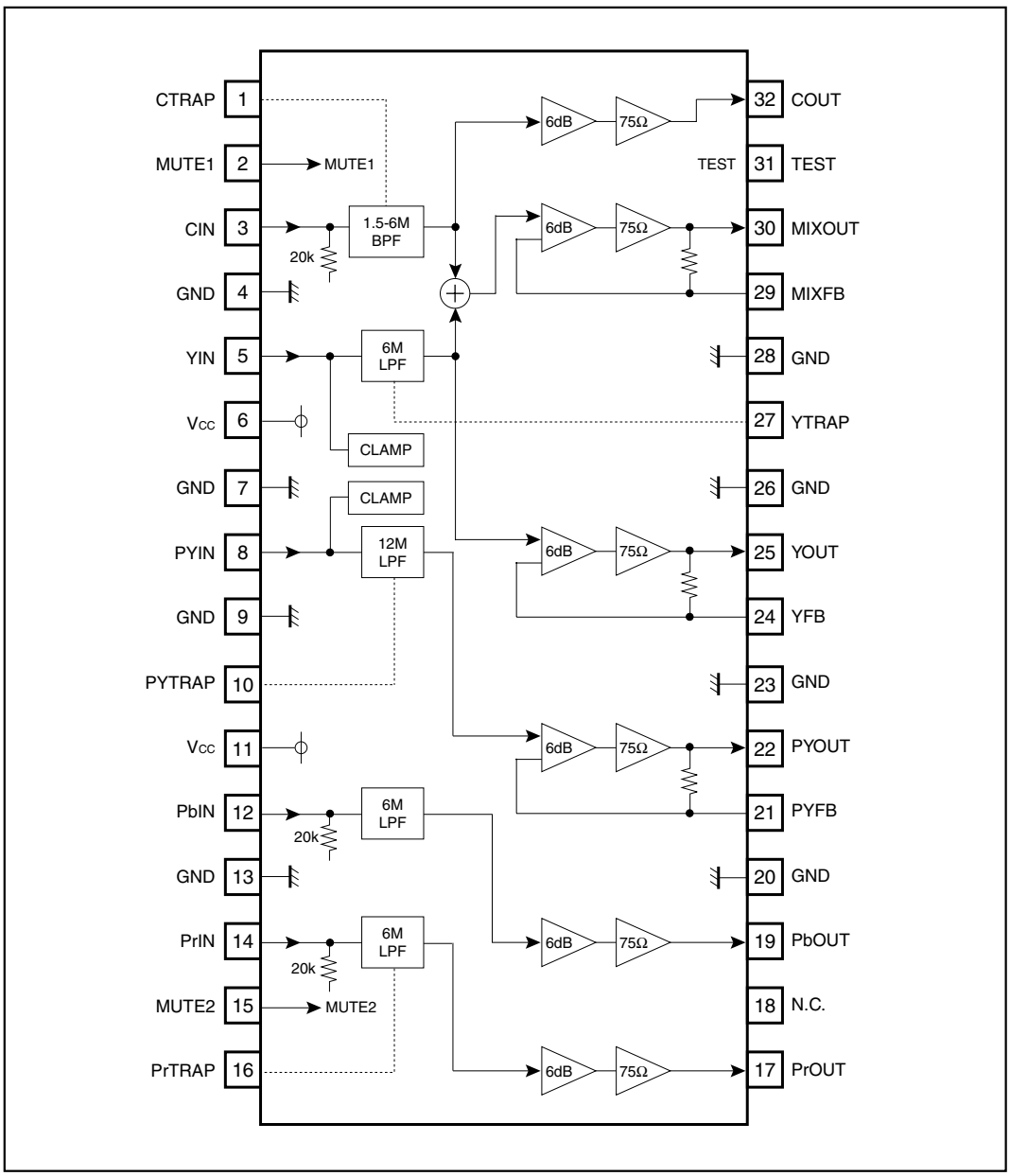
* Reduced by −7.6mW for each increase in Ta of 1°C over 25°C.
PCB (70mm×70mm, t=1.6mm) glass epoxy mounting.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	−	5.5	V

◎Radiation resistance is not included in the design.

●Block diagram



KEC

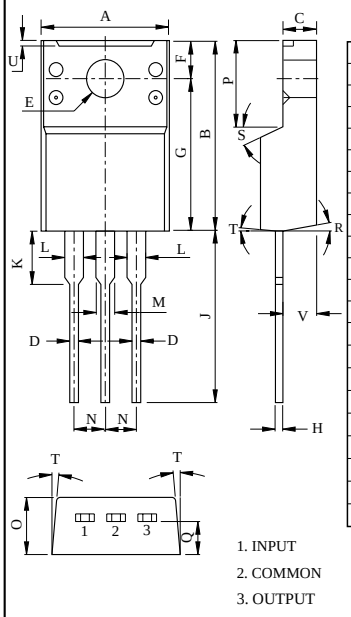
SEMICONDUCTOR
TECHNICAL DATA

KIA7805API~ KIA7824API
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.

FEATURES

· Suitable for C-MOS, TTL, the Other Digital IC's Power Supply.
· Internal Thermal Overload Protection.
· Internal Short Circuit Current Limiting.
· Output Current in Excess of 1A.
· Satisfies IEC-65 Specification. (International Electronical Commission)



DIM	MILLIMETERS
A	10.30 MAX
B	15.30 MAX
C	2.70±0.30
D	0.85 MAX
E	Φ3.20±0.20
F	3.00±0.30
G	12.30 MAX
H	0.75 MAX
J	13.60±0.50
K	3.90 MAX
L	1.20
M	1.30
N	2.54
O	4.50±0.20
P	6.80
Q	2.60±0.20
R	10°
S	25°
T	5°
U	0.5
V	2.60±0.15

TO-220IS

MAXIMUM RATINGS (Ta=25℃)

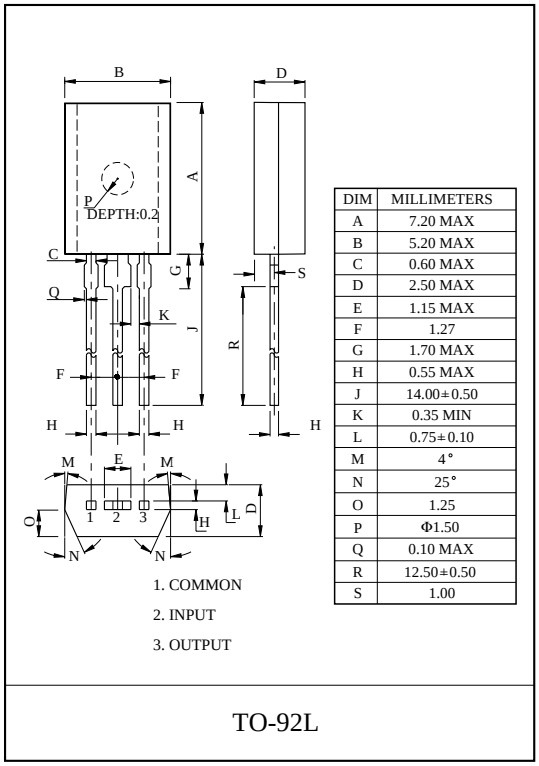
CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA7805API ~ KIA7815API	V_{IN}	35	V
	KIA7818API ~ KIA7824API		40	
Power Dissipation (Tc=25℃)		P_D	20.8	W
Power Dissipation (Without Heatsink)	KIA7805API ~ KIA7824API	P_D	2.0	W
Operating Junction Temperature		T_j	-30 ~150	℃
Storage Temperature		T_{stg}	-55 ~150	℃

KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA79L05BP~ KIA79L24BP
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	7.20 MAX
B	5.20 MAX
C	0.60 MAX
D	2.50 MAX
E	1.15 MAX
F	1.27
G	1.70 MAX
H	0.55 MAX
J	14.00±0.50
K	0.35 MIN
L	0.75±0.10
M	4°
N	25°
O	1.25
P	Φ1.50
Q	0.10 MAX
R	12.50±0.50
S	1.00

TO-92L

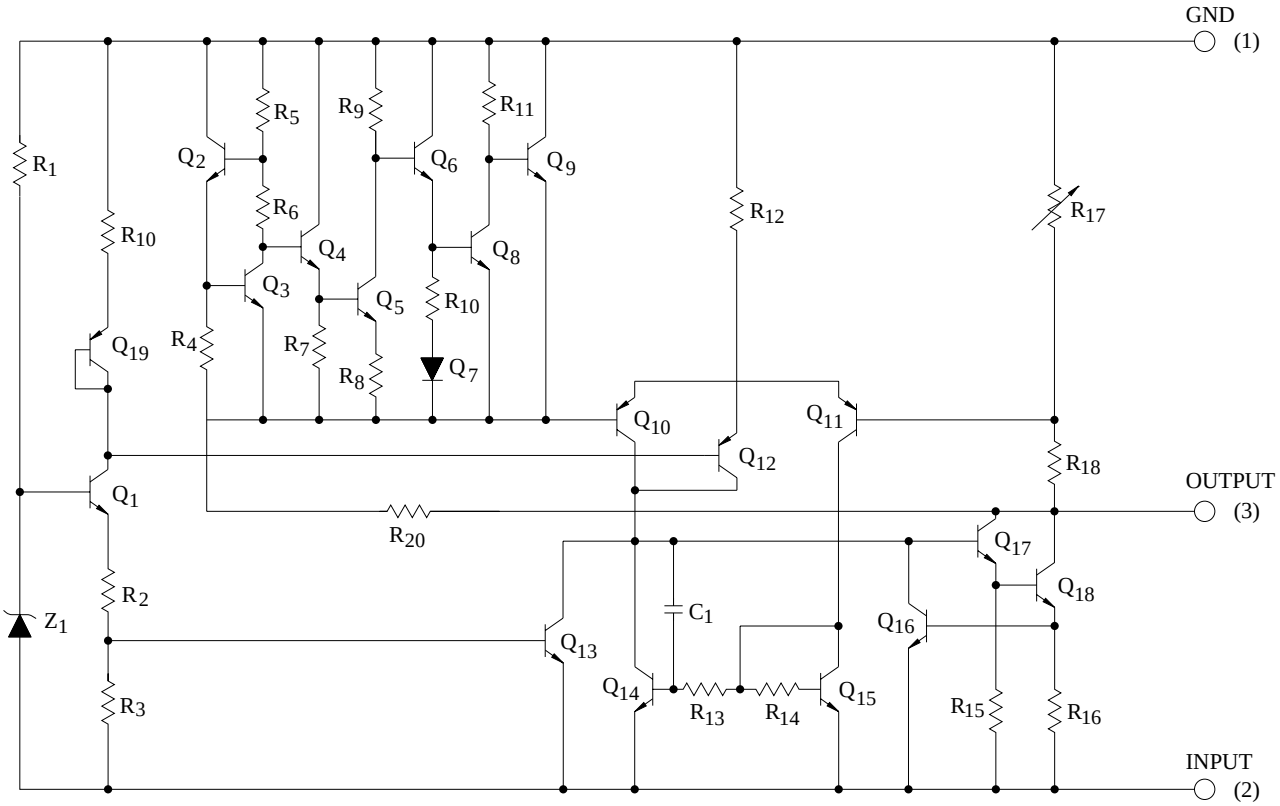
FEATURES

- Best Suited to a Power Supply for TTL and CMOS.
- Built-in Overcurrent Protective Circuit.
- Built-in Thermal Protective Circuit.
- Max. Output Current 150mA (T_j=25℃).
- Packaged in TO-92L.

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA79L05BP ~ KIA79L15BP	V_{IN}	-35	V
	KIA79L18BP ~ KIA79L24BP		-40	
Power Dissipation (Tc=25℃)		P_D	800	mW
Operating Junction Temperature		T_j	-30 ~ 150	℃
Operating Temperature		T_{opr}	-30 ~ 75	℃
Storage temperature		T_{stg}	-55 ~ 150	℃

EQUIVALENT CIRCUIT



Optic receiver modules

KODENSHI

KSM - 60 钡 TH2 · KSM - 70 钡 TH2

The KSM - 60钡TH2 consist of a PIN Photodiode of high speed and a preamplifier IC in the package as an receiver for Infrared remote control systems

FEATURES

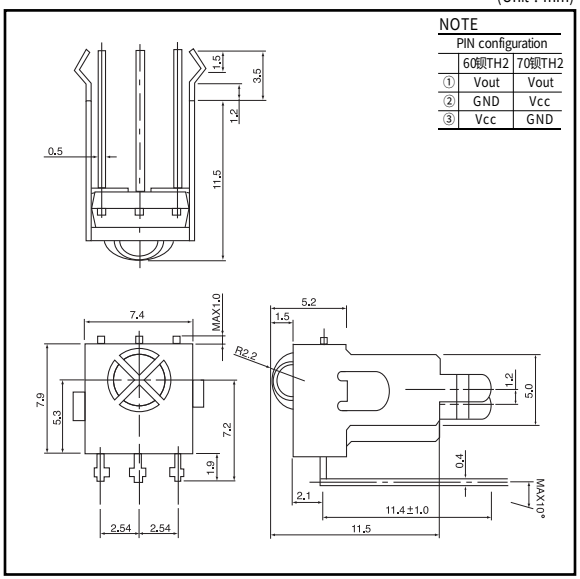
- One mold small package
- 5 Volt supply voltage, low power consumption
- Shielded against electrical field disturbance
- High immunity against ambient light
- Easy interface with the main board
- TTL and CMOS compatibility

APPLICATIONS

- TV, VTR, Acoustic Devices, Air Conditioners, Car Stereo Units, Computers, Interior controlling appliances, and all appliances that require remote controlling

DIMENSIONS

(Unit : mm)



MAXIMUM RATINGS

(Ta=25℃ Unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5.5	V
Operating Temperature	Topr.	- 10~+60	℃
Storage Temperature	Tstg.	- 20~+75	℃
Soldering Temperature	Tsol.	260(Max 5 sec)	℃

B.P.F CENTER FREQUENCY

Model NO.	B.P.F Center Frequency(kHz)
KSM - ◯◯1 TH2	40.0
KSM - ◯◯2 TH2	36.7
KSM - ◯◯3 TH2	37.9
KSM - ◯◯4 TH2	32.7
KSM - ◯◯5 TH2	56.9

ELECTRO-OPTICAL CHARACTERISTICS

(Ta=25℃), Vcc=5.0V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit.
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Current Consumption	I_{CC}	Input Signal=0		-	1.2	2.5	mA
Peak Wavelength *1	λp			-	940	-	nm
B.P.F Center Frequency	fo			-	37.9	-	kHz
Transmission Distance *1	L	200±50lx	0°	10	-	-	m
			±30°	7	-	-	m
H Level Output Voltage *1	V_{OH}	30cm over the ray axis		4.5	5.0	-	V
L Level Output Voltage *1	V_{OL}			-	0.1	0.5	V
H Level Output Pulse Width *1	T_{WH}	Burst Wave=600μs Period=1.2ms		500	600	700	μs
L Level Output Pulse Width *1	T_{WL}			500	600	700	μs
Output Form				Active Low Output			

Note : *1. It specifies the maximum distance between emitter and detector that the output waveform satisfies the standard under the conditions below against the standard transmitter

1) Measuring place : Indoor without extreme reflection of light
2) Ambient light source : Detecting surface illumination shall be irradiate 200±50lx under ordinary white fluorescence lamp without high frequency lightning
3) Standard transmitter : Burst wave of standard transmitter shall be arranged to 50mVp - p under the measuring circuit

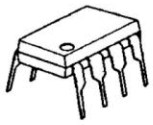
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate, which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

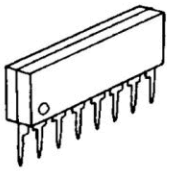
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V

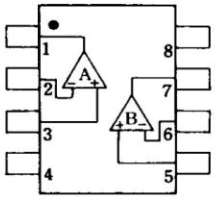


NJM2068L

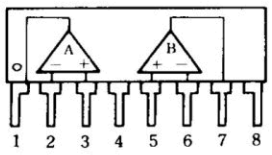
■ FEATURES

● Operating Voltage	(±4V~±18V)
● Low Total Harmonic Distortion	(0.001% typ.)
● Low Noise Voltage	(FLAT+JISA,0.56μV typ.)
● High Slew Rate	(6V/μs typ.)
● Unity Gain Bandwidth	(27MHz @ f=10kHz)
● Package Outline	DIP8,DMP8,SIP8,SSOP8
● Bipolar Technology	

■ PIN CONFIGURATION



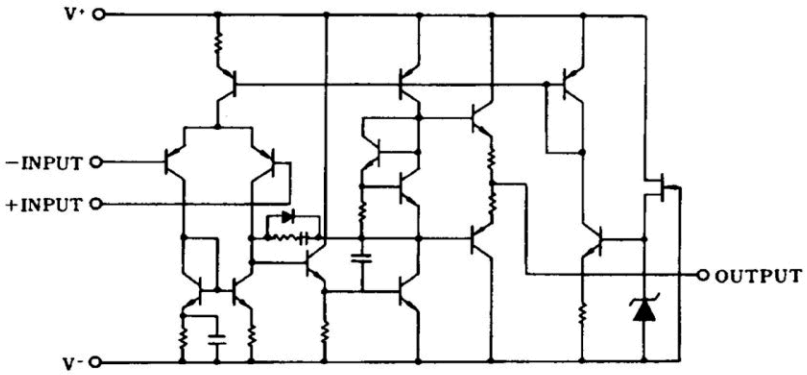
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V^-
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)



National Semiconductor

October 2002

LM1117/LM1117I
800mA Low-Dropout Linear Regulator

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

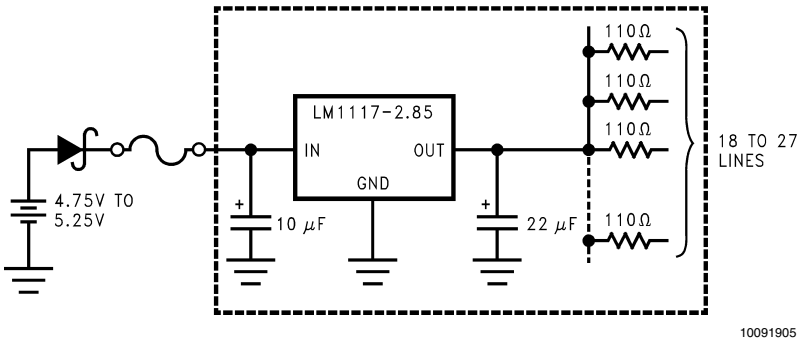
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0˚C to 125˚C
  - — LM1117I –40˚C to 125˚C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

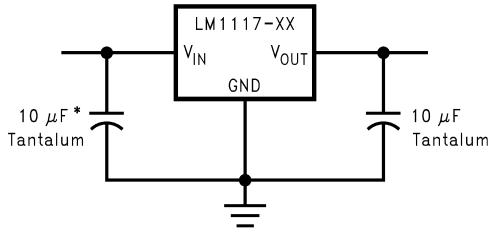
Typical Application

Active Terminator for SCSI-2 Bus



10091905

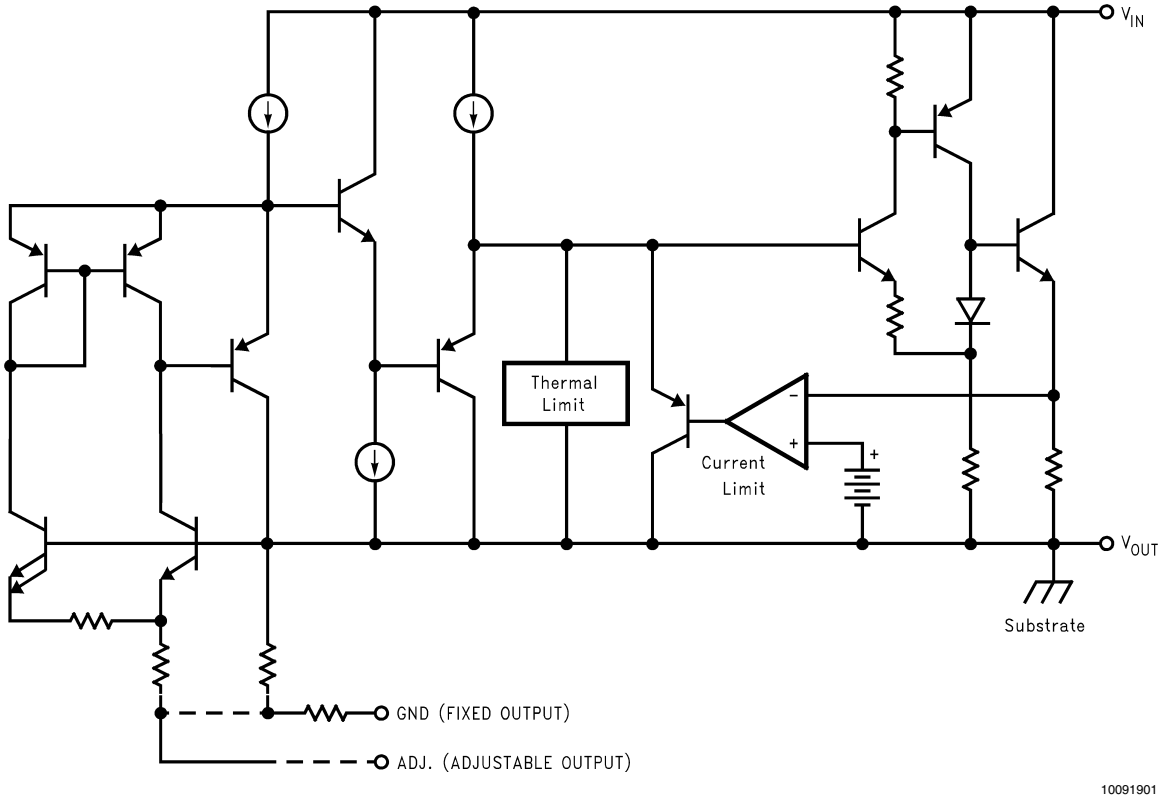
Fixed Output Regulator



* Required if the regulator is located far from the power supply filter.

10091928

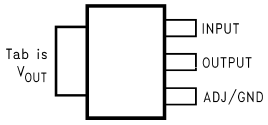
Block Diagram



10091901

Connection Diagrams

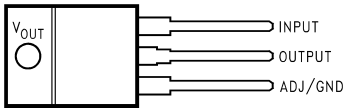
SOT-223



10091904

Top View

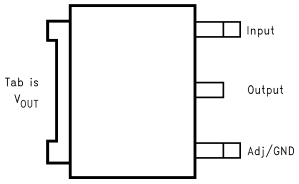
TO-220



10091902

Top View

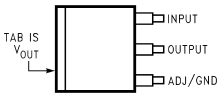
TO-252



10091938

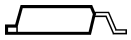
Top View

TO-263



10091944

Top View



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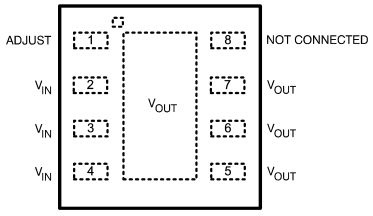
Side View

LLP



10091946

When using the LLP package
Pins 2, 3 & 4 must be connected together and
Pins 5, 6 & 7 must be connected together

Top View

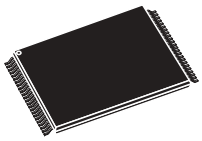
M29W160ET
M29W160EB

16 Mbit (2Mb x8 or 1Mb x16, Boot Block) 3V Supply Flash Memory

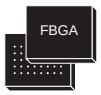
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
- ACCESS TIMES: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
- 35 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom Location)
  - 2 Parameter and 32 Main Blocks
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte/Word Program algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29W160ET: 22C4h
  - Bottom Device Code M29W160EB: 2249h

Figure 1. Packages



TSOP48 (N)
12 x 20mm



TFBGA48 (ZA)
6 x 8mm

SUMMARY DESCRIPTION

The M29W160E is a 16 Mbit (2Mb x8 or 1Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Figures 5 and 6, Block Addresses. The first or last 64 KBytes have been divided into four additional blocks. The 16 KByte Boot Block can be used for small initialization code to start the microprocessor, the two 8 KByte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered TSOP48 (12 x 20mm) and TFBGA48 (0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

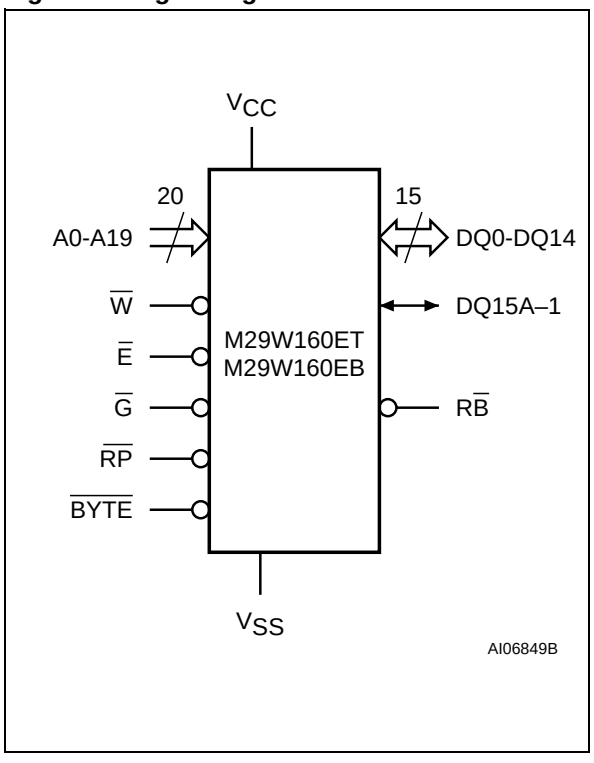
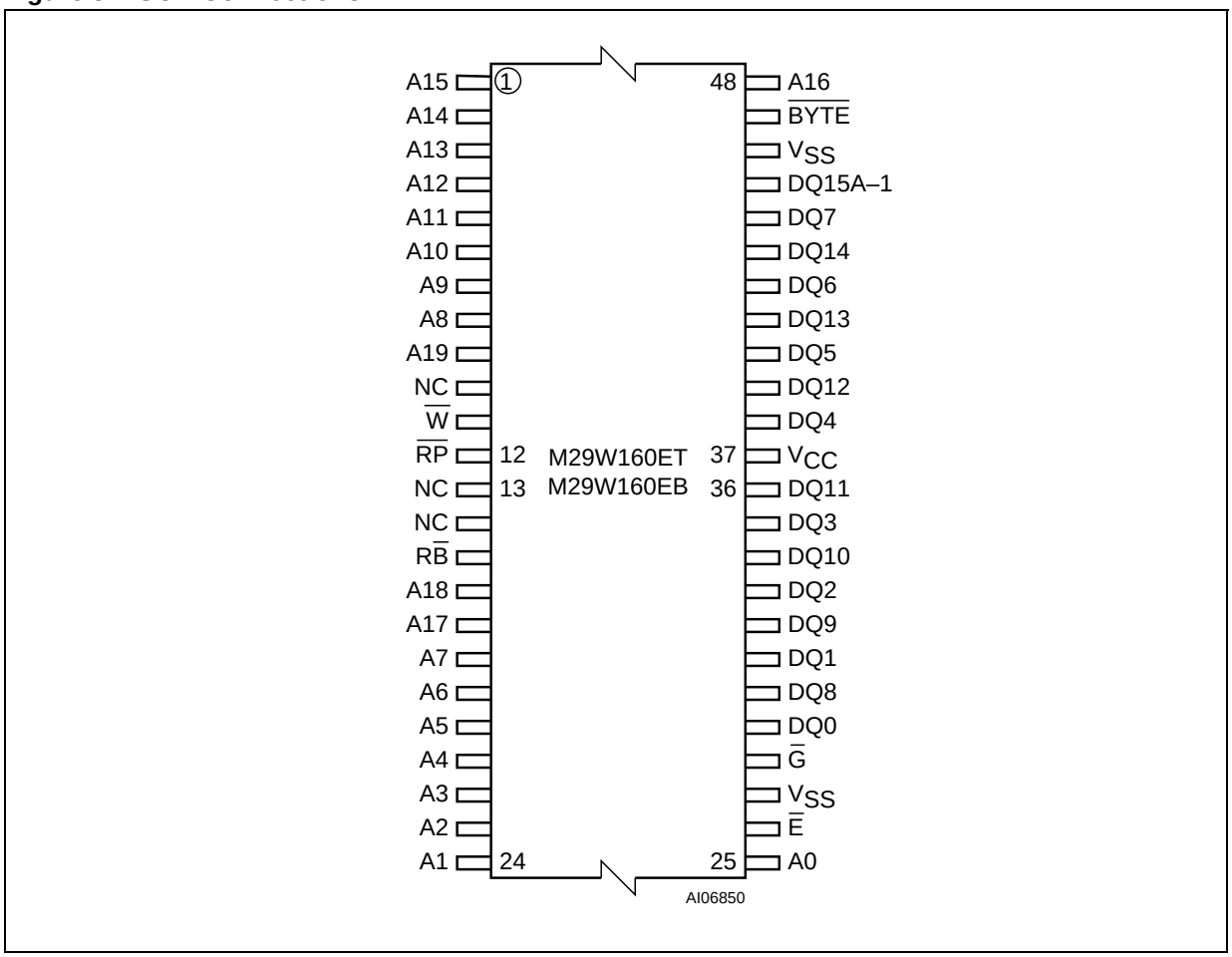


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections



SAA7893HL

Super audio media player

Rev. 02 — 26 February 2003 **Product data**

1. General description

Thanks to the superior sound quality and multichannel capability of Super Audio CD (SACD) technology, multimedia devices such as DVD players and home cinema systems are incorporating SACD functionality. Philips' Super Audio Media Player (SA-MP) provides a flexible, state-of-the-art solution for SACD playback on DVD architectures.

Built around the SAA7893HL SACD processor, SA-MP system solution delivers complete SACD functionality, avoiding the need for continual redesign and re-integration of SACD into various applications. The system is completed with a single 64 Mbit SDRAM and has extensive software processing options, resulting in low total system cost (see Figure 1).

With integrated support for multiple loaders, the SAA7893 supports a variety of DVD platforms. High level and standard software interfaces – optimized for easy design-in – further enhance adaptability, enabling designers to build SACD players on many different hardware and software platforms. This ensures that the SA-MP can be left unchanged even if the SACD playback hardware is altered, again minimizing development effort.

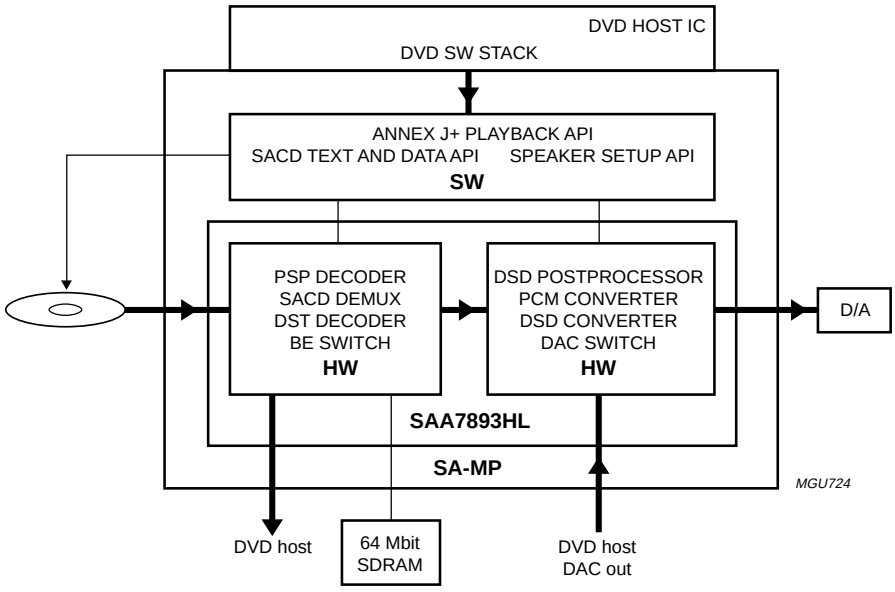


Fig 1. General block diagram.

1.1 Hardware

The SA-MP hardware consists of the SAA7893HL device. A typical HW block diagram of a DVD system incorporating the SAA7893HL is shown in Figure 2.

The SAA7893HL takes sector data from the front-end. The front-end is controlled by the DVD host via the SA-MP software stack. The SAA7893HL uses one 64 Mbit SDRAM for audio data buffering and storage of SACD TOCs. The front-end timing can be fully asynchronous from all clocks.

The 6-channel DAC outputs of the DVD host are routed via the SAA7893HL which provides a DAC switch function between SACD mode and DVD mode. The audio outputs of the SAA7893HL operate on the system audio clock.

The DVD back-end communicates with the SAA7893HL via a host bus. The system clock and the system audio clock are allowed to be asynchronous.

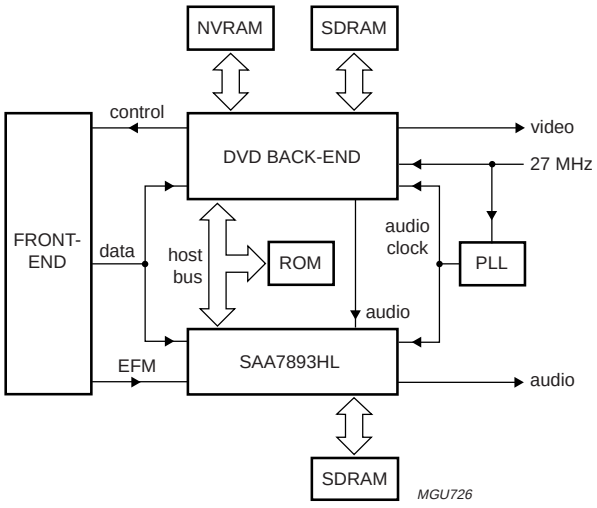


Fig 2. Hardware block diagram.

1.2 Software

The SA-MP software is delivered in the form of a library in the development environment of the DVD host. The SA-MP software has been developed in ANSI-C using conventional software technology to allow easy integration into any development environment. A typical software block diagram of a DVD system incorporating SA-MP is shown in Figure 3.

At the device driver and HW-level, SA-MP interfaces with the SAA7893HL and a front-end driver. At the infrastructure level, SA-MP interfaces with an Operating System Abstraction layer (OSA). At the application level, SA-MP provides a high-level playback and post-processing interface which is easy to integrate into typical applications.

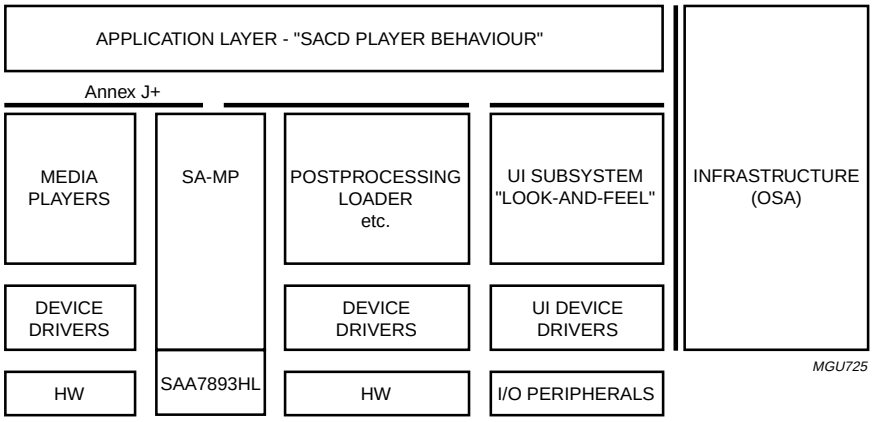


Fig 3. Software block diagram.

2. Features

2.1 Components

- SAA7893HL second generation SACD processor IC
- SA-MP Annex J+ level software stack.

2.2 HW interfaces

- Front-end, supports 3 types:
  - UDE
  - FEC
  - I^2S-bus
- Flexible PSP detection from EFM signal with AGC, without EFM clock (digital PLL)
- (DVD-)host bus, supports 3 types:
  - Separate address/data bus (SAD16) with 16-bit data bus (3 different modes)
  - Multiplexed address/data bus (MAD16) with 16-bit data bus (2 different modes)
  - Separate address/data bus (SAD08) with 8-bit data bus (1 mode)
- 16-bit 100 MHz SDRAM interface supports one 64 Mbit device
- 6-channel I^2S-PCM audio input 44.1, 48, 88.2, 96, 176.4 or 192 kHz at 16-bit or 24-bit
- 6-channel DSD or I^2S-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- 2-channel DSD or I^2S-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- Audio clock reference $256f_s$, $384f_s$, $512f_s$ or $768f_s$
- System clock 27 to 35 MHz.

2.3 SW interfaces

- Annex J+ level playback interface

- High-level audio post-processing control
- SACD data interface
- System configuration

2.4 System

- Full SACD Menu TOC and Area TOC storage in VBR
- Front-end clock asynchronous to other clocks

2.5 System configuration

- D/A converters:
  - DSD and PCM selectable pin sharing configuration
  - DSD clock polarity
- Audio and system clock asynchronous
- Front-end type

2.6 SACD playback

- SACD playback:
  - Multi-channel
  - 2-channel
- PSP processing
- Decrypting and demultiplexing
- VBR management
- DST decoding
- Fade processing
- Annex J+ level software interface:
  - Stop
  - Pause
  - Play
  - Fast forward
  - Fast reverse
  - Next/previous track
  - Program and play playlist
  - Repeat (Track, All or AB)
  - Shuffle
  - Introscan
  - Time search

2.7 Audio postprocessing

- DSD Bass Management with support of:
  - Dolby® configuration 0 (LLL1)
  - Dolby® configuration 1 (SSS1)
  - Dolby® configuration 2 (LSS0)
- Programmable bass filter frequency and slope:

- 60, 80, 100, 120 Hz
- 12, 18, 24 dB/Oct

(other frequencies or slopes are possible on customer request)

- DSD down mixing:
  - 2/2
  - 3/0
  - 2/0
  - separate 2/0
- DSD attenuation function 0 to −90 dB, programmable per channel
- DSD delay function total 65 ms (approximately 20 meters), programmable per channel
- 6-channel PCM input:
  - 44.1, 88.2, 176.4, 48, 96 or 192 kHz at 16-bit or 24-bit
  - PCM to DSD upsampling with 3 programmable Sigma-Delta and anti-aliasing filter modes
  - Attenuation and delay as with DSD
- DSD to PCM conversion 88.2, 176.4 kHz at 24-bit.

2.8 SACD data and text

- Album info
- Disc info
- Album or disc text
- Area text
- Track data
- Track text.

2.9 General

- E-JTAG for board test and debug
- 3.3 V pad supply voltage
- 1.8 V core supply voltage
- 1.8 V analog supply voltage
- LQFP128 package
- 0.18 µm CMOS process.

3. Applications

- Consumer DVD players
- Home cinema
- Car audio systems.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SAA7893HL	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm^2	SOT425-1

5. Block diagram

Figure 4 shows the block diagram of the SAA7893HL with all defined functions.

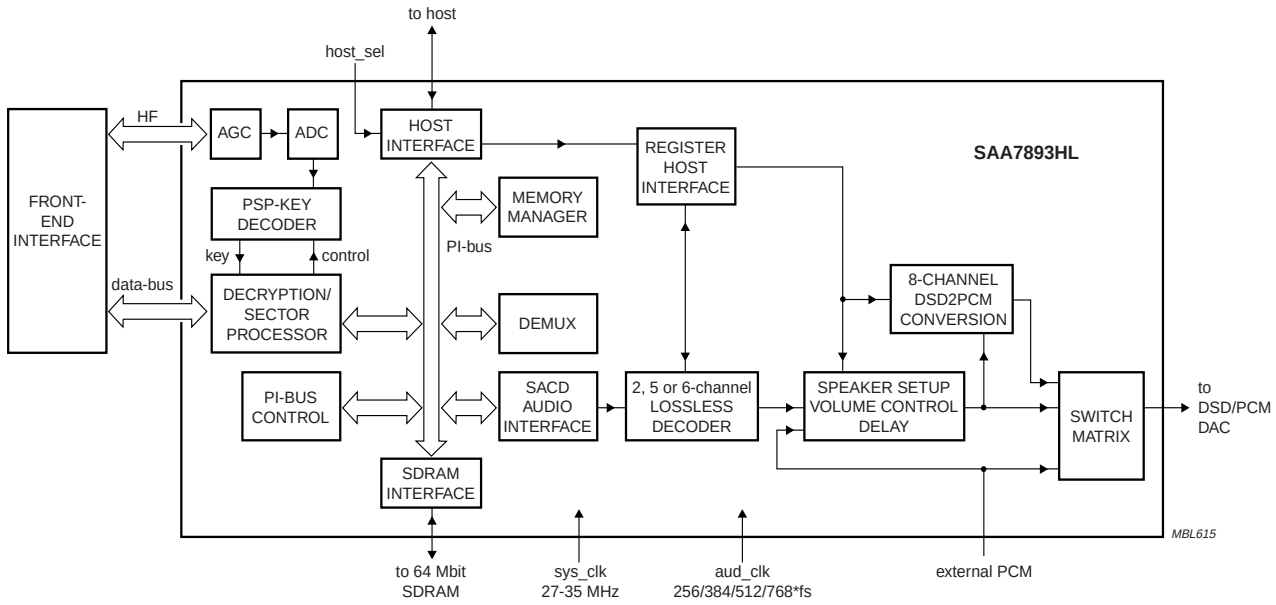


Fig 4. Block diagram.

6. Pinning information

6.1 Pinning

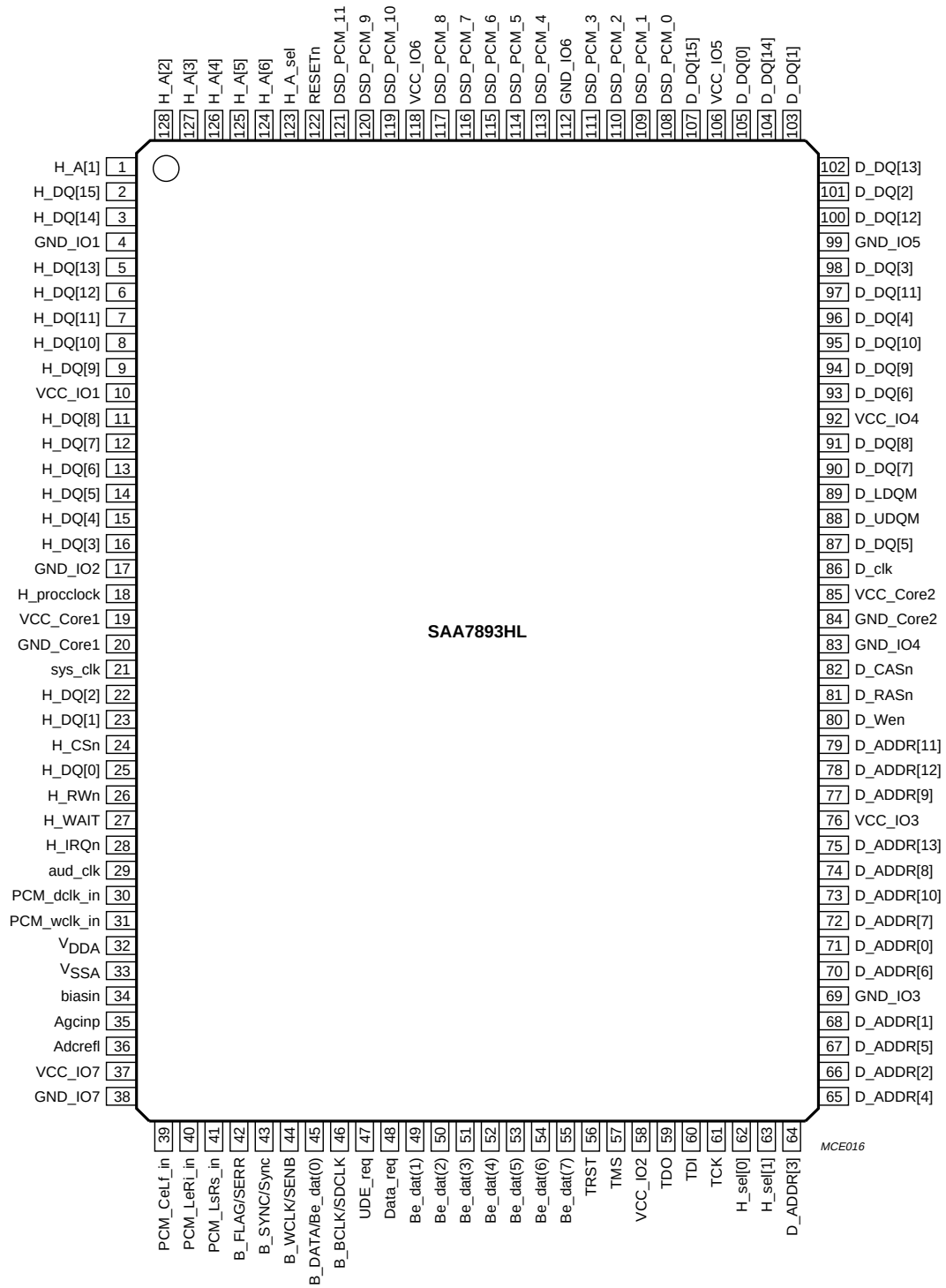


Fig 5. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Type[1]	Description
H_A[1]	1	IN	address bus
H_DQ[15]	2	I/O10	data bus
H_DQ[14]	3	I/O10	data bus
GND_IO1	4	GND_IO	GND I/O pads
H_DQ[13]	5	I/O10	data bus
H_DQ[12]	6	I/O10	data bus
H_DQ[11]	7	I/O10	data bus
H_DQ[10]	8	I/O10	data bus
H_DQ[9]	9	I/O10	data bus
VCC_IO1	10	VCC_IO	V_{CC} I/O pads
H_DQ[8]	11	I/O10	data bus
H_DQ[7]	12	I/O10	data bus
H_DQ[6]	13	I/O10	data bus
H_DQ[5]	14	I/O10	data bus
H_DQ[4]	15	I/O10	data bus
H_DQ[3]	16	I/O10	data bus
GND_IO2	17	GND_IO	GND I/O pads
H_procclock	18	IN	host processor EMI interface clock
VCC_Core1	19	VCC_core	core supply voltage
GND_Core1	20	GND_core	core ground
sys_clk	21	IN	system clock
H_DQ[2]	22	I/O10	data bus
H_DQ[1]	23	I/O10	data bus
H_CSn	24	IN	host chip select; active LOW
H_DQ[0]	25	I/O10	data bus
H_RWn	26	IN	read = 1; write = 0
H_WAIT	27	O10	wait signal
H_IRQn	28	O10	interrupt request; active LOW
aud_clk	29	IN	DSD audio clock
PCM_dclk_in	30	IN	PCM data clock
PCM_wclk_in	31	IN	PCM word clock
V_{DDA}	32	VDDCO	V_{DD} of ADC
V_{SSA}	33	VSSCO	V_{SS} of AGC and ADC; connected to substrate
biasin	34	APIO	bias current input
Agcinp	35	APIO	AGC positive input signal; HF in
Adcrefl	36	APIO	ADC decoupling
VCC_IO7	37	VCC_IO	V_{CC} I/O pads
GND_IO7	38	GND_IO	GND I/O pads
PCM_CeLf_in	39	IN	PCM data center or LFE

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
PCM_LeRi_in	40	IN	PCM data left or right
PCM_LsRs_in	41	IN	PCM data left or right surround
B_FLAG/SERR	42	IN	I^2S-bus flag (EDC flag)
B_SYNC/Sync	43	IN	sector sync or absolute time sync
B_WCLK/SENB	44	IN	I^2S-bus word clock or UDE data sense from host
B_DATA/Be_dat(0)	45	IN	I^2S-bus data or LSB data of parallel interface
B_BCLK/SDCLK	46	IN	I^2S-bus bit clock
UDE_req	47	IN	host request data from front-end; routed via the SAA7893HL
Data_req	48	O10	data request for UDE
Be_dat(1)	49	IN	front-end parallel data interface
Be_dat(2)	50	IN	front-end parallel data interface
Be_dat(3)	51	IN	front-end parallel data interface
Be_dat(4)	52	IN	front-end parallel data interface
Be_dat(5)	53	IN	front-end parallel data interface
Be_dat(6)	54	IN	front-end parallel data interface
Be_dat(7)	55	IN	front-end parallel data interface
TRST	56	IN1	boundary scan reset
TMS	57	IN1	boundary scan mode select
VCC_IO2	58	VCC_IO	V_{CC} I/O pads
TDO	59	O10	output
TDI	60	IN1	boundary scan data input
TCK	61	IN	boundary scan clock
H_sel[0]	62	IN	host select signals: SAD16, MAD16 and SAD08
H_sel[1]	63	IN	host select signals: SAD16, MAD16 and SAD08
D_ADDR[3]	64	O10	SDRAM address bus
D_ADDR[4]	65	O10	SDRAM address bus
D_ADDR[2]	66	O10	SDRAM address bus
D_ADDR[5]	67	O10	SDRAM address bus
D_ADDR[1]	68	O10	SDRAM address bus
GND_IO3	69	GND_IO	GND I/O pads
D_ADDR[6]	70	O10	SDRAM address bus
D_ADDR[0]	71	O10	SDRAM address bus
D_ADDR[7]	72	O10	SDRAM address bus
D_ADDR[10]	73	O10	SDRAM address bus
D_ADDR[8]	74	O10	SDRAM address bus
D_ADDR[13]	75	O10	SDRAM address bus
VCC_IO3	76	VCC_IO	V_{CC} I/O pads
D_ADDR[9]	77	O10	SDRAM address bus

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
D_ADDR[12]	78	O10	SDRAM address bus
D_ADDR[11]	79	O10	SDRAM address bus
D_Wen	80	O10	read or write
D_RASn	81	O10	row address select; active LOW
D_CASn	82	O10	column address select; active LOW
GND_IO4	83	GND_IO	GND I/O pads
GND_Core2	84	GND_core	core ground
VCC_Core2	85	VCC_core	core supply voltage
D_clk	86	O10	clock signal needed for SDRAM
D_DQ[5]	87	I/O10	data bus
D_UDQM	88	O10	DQ mask enable (upper)
D_LDQM	89	O10	DQ mask enable (lower)
D_DQ[7]	90	I/O10	data bus
D_DQ[8]	91	I/O10	data bus
VCC_IO4	92	VCC_IO	V_{CC} I/O pads
D_DQ[6]	93	I/O10	data bus
D_DQ[9]	94	I/O10	data bus
D_DQ[10]	95	I/O10	data bus
D_DQ[4]	96	I/O10	data bus
D_DQ[11]	97	I/O10	data bus
D_DQ[3]	98	I/O10	data bus
GND_IO5	99	GND_IO	GND I/O pads
D_DQ[12]	100	I/O10	data bus
D_DQ[2]	101	I/O10	data bus
D_DQ[13]	102	I/O10	data bus
D_DQ[1]	103	I/O10	data bus
D_DQ[14]	104	I/O10	data bus
D_DQ[0]	105	I/O10	data bus
VCC_IO5	106	VCC_IO	V_{CC} I/O pads
D_DQ[15]	107	I/O10	data bus
DSD_PCM_0	108	O10	6-channel data output
DSD_PCM_1	109	O10	6-channel data output
DSD_PCM_2	110	O10	6-channel data output
DSD_PCM_3	111	O10	6-channel data output
GND_IO6	112	GND_IO	GND I/O pads
DSD_PCM_4	113	O10	6-channel data output
DSD_PCM_5	114	O10	6-channel data output
DSD_PCM_6	115	O10	6-channel clock/control
DSD_PCM_7	116	O10	6-channel clock/control
DSD_PCM_8	117	O10	2-channel clock/control
VCC_IO6	118	VCC_IO	V_{CC} I/O pads

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
DSD_PCM_10	119	O10	2-channel data output
DSD_PCM_9	120	O10	2-channel clock or control
DSD_PCM_11	121	O10	2-channel data output
RESETn	122	IN	asynchronous reset; active LOW
H_A_sel	123	IN	address select
H_A[6]	124	IN	address bus
H_A[5]	125	IN	address bus
H_A[4]	126	IN	address bus
H_A[3]	127	IN	address bus
H_A[2]	128	IN	address bus

[1] Explanation of input and output ports:
IN: digital input port; all dedicated inputs are TTL tolerant.
IN1: digital input port with internal pull-up resistor.
I/O10: bidirectional port with 10 ns slew rate.
O10: 3-state (in test mode) output port with 10 ns slew rate.
APIO: analog input port.
VDDCO: analog V_{DD} port (1.8 V).
VSSCO: analog V_{SS} port.
GND_IO: ground for I/O pads.
VCC_IO: V_{CC} for I/O pads (3.3 V).
GND_core: ground for core.
VCC_core: V_{CC} for core (1.8 V).

7. Interfaces

7.1 Host interface

Different types of host busses are supported:

- Separate address/data bus with 16-bit data bus (3 different modes)
- Multiplexed address/data bus with 16-bit data bus (2 different modes)
- Separate address/data bus with 8-bit data bus (1 mode).

The host interface type is set via the dedicated pins H_sel and sys_clk. The SAA7893HL has a dedicated interrupt output pin.

7.2 Front-end interface

7.2.1 Data input interface

The SAA7893HL supports three different front-end interfaces which are selectable via the host interface:

- I^2S-bus interface: the front-end interface is in essence an I^2S-bus interface and therefore, it has to conform to the I^2S-bus specification.
- FEC interface

- Parallel interface (UDE data interface part): a parallel front-end interface with a handshake protocol.

7.2.2 Analog HF input

The analog HF input, coming from the optical pickup unit, is also fed to the SAA7893HL to extract the copy protection information PSP.

7.3 Audio interface

7.3.1 Audio input

The audio input is a 6-channel PCM-I^{2}S input.

7.3.2 DAC interface

The audio output is a 6-channel output and a separate stereo output. Both outputs can be set in DSD and in PCM-I^{2}S mode.

7.4 SDRAM interface

The SDRAM interface forms a glueless interface to one 64 Mbit SDRAM device.

Supported devices are only PC100 compliant or faster SDRAM devices:

- Organization: 64 Mbit (1M $\times$ 16 $\times$ 4 banks)
- Refresh period: 4096 cycles per 64 ms
- Clock frequency: $f_{clk} \geq 100$ MHz
- Refresh cycle: $t_{rcar} \leq 70$ ns
- Command period: $t_{rc} \leq 70$ ns.

7.5 Clock and reset input

Different processing clocks are needed in the SAA7893HL:

- sys_clk: system clock for data processing part; frequency can be between 27 and 35 MHz; see Figure 6 and Table 3
- aud_clk: audio clock reference; can be 256/384/512/768 $\times$ f_s (f_s = 44.1 to 48 kHz); see Figure 7 and Table 4
- proc_clk: host processor clock (only used in SAD16_01/02 mode)
- B_BCLK: front-end bit/byte clock.

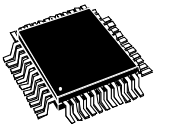
It is not required that these clocks are locked.

RESETn is an asynchronous reset and should be kept LOW for at least 10 periods of sys_clk.

ST72F324L, ST72324BL

3V RANGE 8-BIT MCU WITH 8 TO 32K FLASH/ROM, 10-BIT ADC, 4 TIMERS, SPI, SCI INTERFACE

- **Memories**
  - 8 to 32K dual voltage High Density Flash (HDFlash) or ROM with read-out protection capability. In-Application Programming and In-Circuit Programming for HDFlash devices
  - 384 to 1K bytes RAM
  - HDFlash endurance: 100 cycles, data retention: 20 years at 55°C
- **Clock, Reset And Supply Management**
  - Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator, and bypass for external clock
  - PLL for 2x frequency multiplication
  - Four Power Saving Modes: Halt, Active-Halt, Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 9/6 external interrupt lines (on 4 vectors)
- **Up to 32 I/O Ports**
  - 32/24 multifunctional bidirectional I/O lines
  - 22/17 alternate function lines
  - 12/10 high sink outputs
- **4 Timers**
  - Main Clock Controller with: Real time base, Beep and Clock-out capabilities
  - Configurable watchdog timer
  - 16-bit Timer A with: 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes
  - 16-bit Timer B with: 2 input captures, 2 output compares, PWM and pulse generator modes



TQFP44
10 x 10

TQFP32
7 x 7

SDIP32
400 mil

- **2 Communication Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface
- **1 Analog Peripheral**
  - 10-bit ADC with up to 12 input ports
- **Instruction Set**
  - 8-bit Data Manipulation
  - 63 Basic Instructions
  - 17 main Addressing Modes
  - 8 x 8 Unsigned Multiply Instruction
- **Development Tools**
  - Full hardware/software development package
  - In-Circuit Testing capability

Device Summary

Features	ST72F324L(J/K)6	ST72F324L(J/K)4	ST72F324L(J/K)2	ST72324BL(J/K)4	ST72324BL(J/K)2
Program memory - bytes	Flash 32K	Flash 16K	Flash 8K	ROM 16K	ROM 8K
RAM (stack) - bytes	1024 (256)	512 (256)	384 (256)	512 (256)	384 (256)
Voltage Range	2.85 to 3.6V				
Temp. Range	up to -40°C to +85°C				
Packages	TQFP44 10x10, SDIP32, TQFP32 7x7				

Rev. 3

1 INTRODUCTION

The ST72F324L and ST72324BL devices are members of the ST7 microcontroller family designed for the 3V operating range. They can be grouped as follows:

– The 32-pin devices are designed for mid-range applications

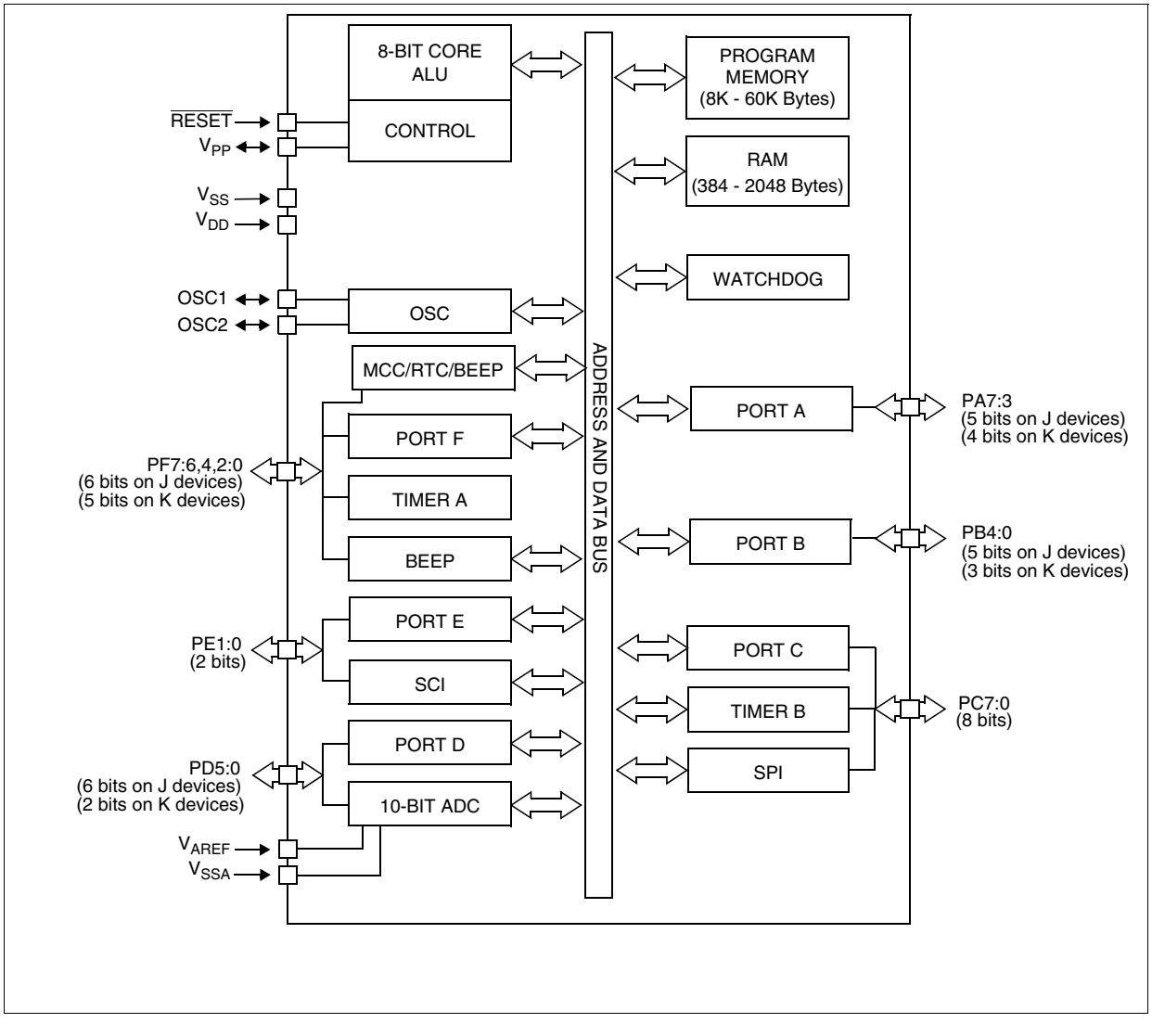
– The 44-pin devices target the same range of applications requiring more than 24 I/O ports.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH or ROM program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

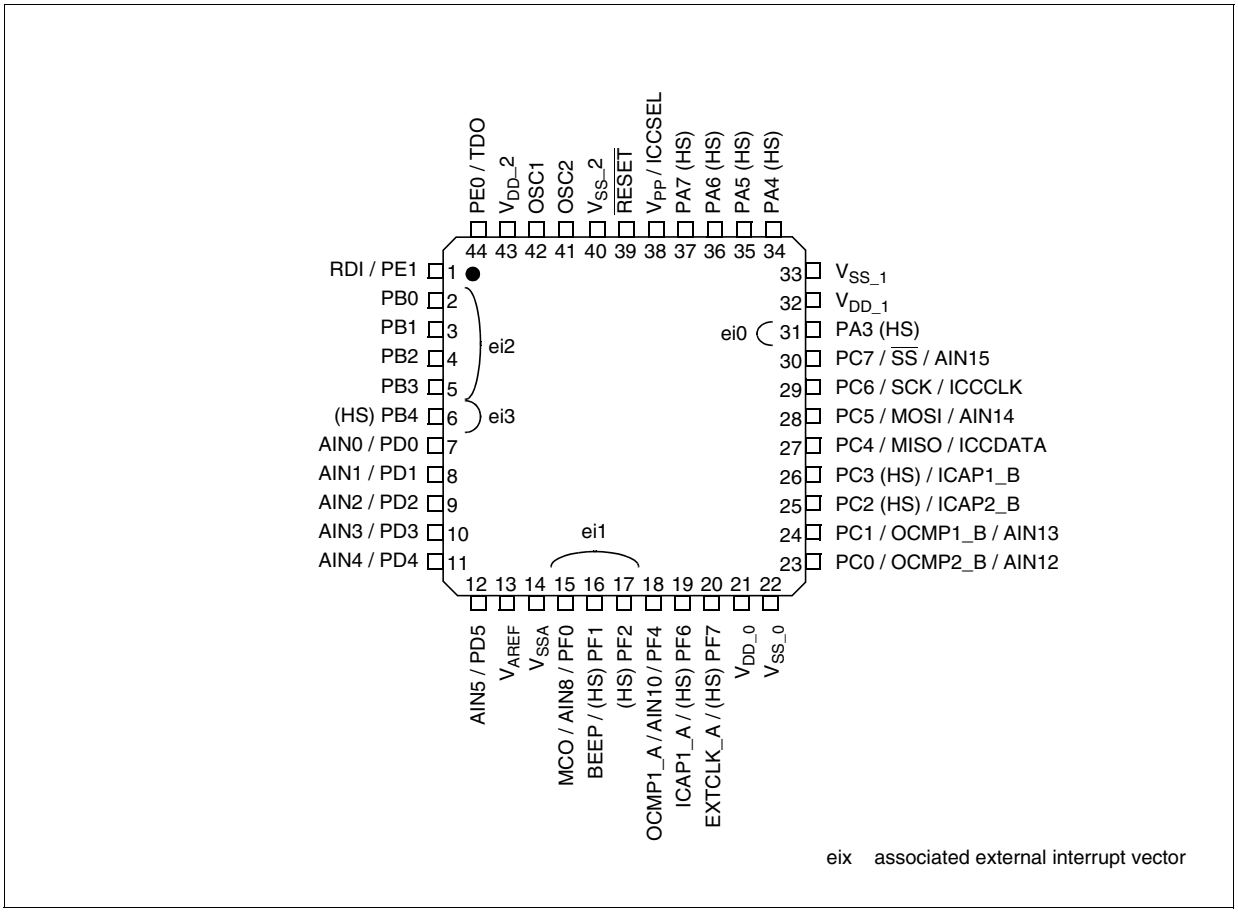
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 44-Pin TQFP Package Pinouts



PIN DESCRIPTION (Cont'd)

Figure 3. 32-Pin SDIP Package Pinout

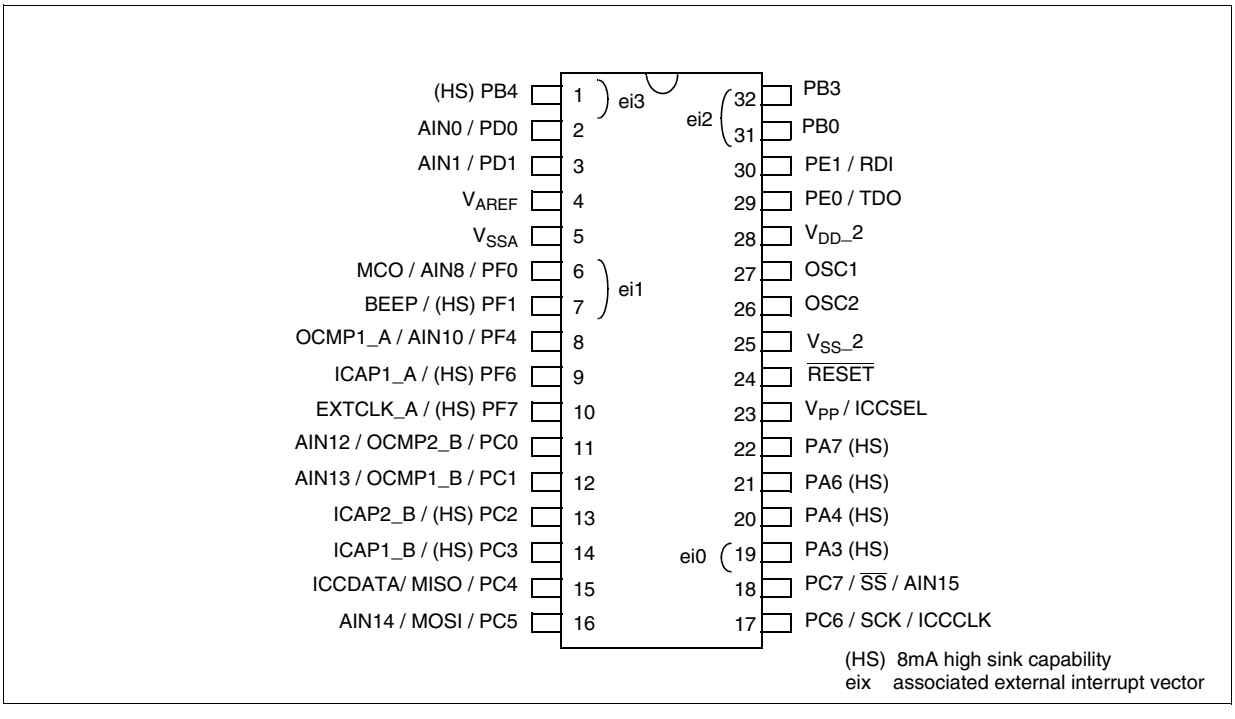
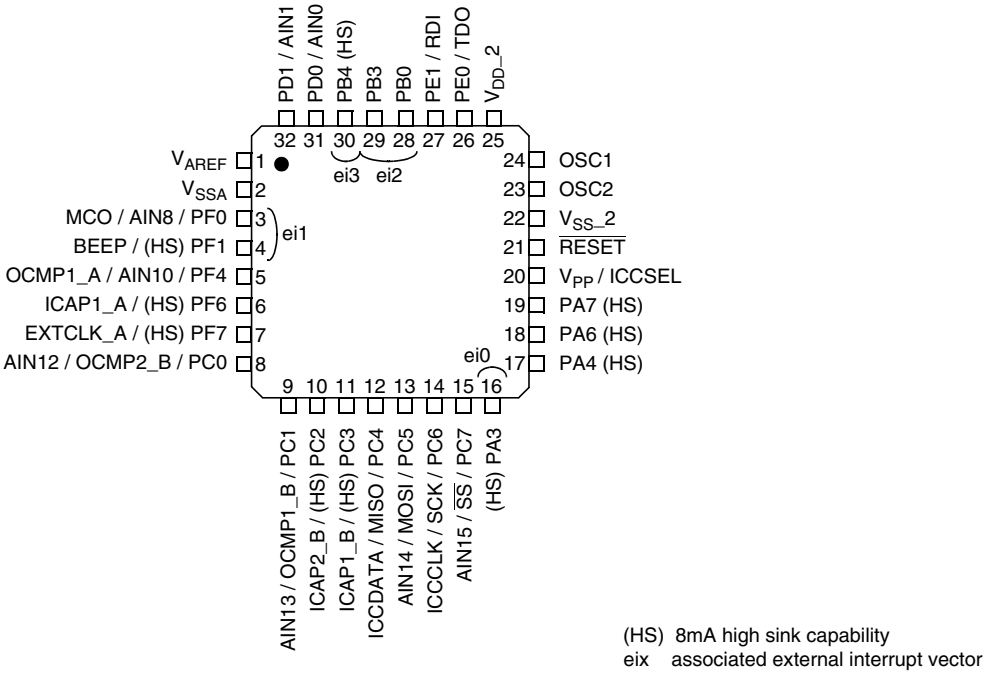


Figure 4. 32-Pin TQFP 7x7 Package Pinout



PIN DESCRIPTION (Cont'd)

For more details, refer to "ELECTRICAL CHARACTERISTICS" on page 110

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

In/Output level: C = CMOS
C_T= CMOS with input trigger

Output level: HS = high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog ports

– Output: OD = open drain [2], PP = push-pull

Refer to "I/O PORTS" on page 39 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
6	30	1	PB4 (HS)	I/O	C_T	HS	**X**	ei3			X	X	Port B4		
7	31	2	PD0/AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0	
8	32	3	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1	
9			PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2	
10			PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3	
11			PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
12			PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
13	1	4	V_{AREF}	S									Analog Reference Voltage for ADC		
14	2	5	V_{SSA}	S									Analog Ground Voltage		
15	3	6	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
16	4	7	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
17			PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
18	5	8	PF4/OCMP1_A/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
19	6	9	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
20	7	10	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
21			V_{DD_0}	S									Digital Main Supply Voltage		
22			V_{SS_0}	S									Digital Ground Voltage		
23	8	11	PC0/OCMP2_B/ AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
24	9	12	PC1/OCMP1_B/ AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
25	10	13	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B Input Capture 2	
26	11	14	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B Input Capture 1	
27	12	15	PC4/MISO/ICCDATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
28	13	16	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
29	14	17	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
30	15	18	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
31	16	19	PA3 (HS)	I/O	C_T	HS	X		ei0		X	X	Port A3		
32			V_{DD_1}	S									Digital Main Supply Voltage		
33			V_{SS_1}	S									Digital Ground Voltage		
34	17	20	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
35			PA5 (HS)	I/O	C_T	HS	X	X			X	X	Port A5		
36	18	21	PA6 (HS)	I/O	C_T	HS	X				T		Port A6 [1)]		
37	19	22	PA7 (HS)	I/O	C_T	HS	X				T		Port A7 [1)]		
38	20	23	V_{PP} /ICCSEL	I									Must be tied low. In the flash programming mode, this pin acts as the programming voltage input V_{PP}. See Section 12.9.2 for more details. High voltage must not be applied to ROM devices.		
39	21	24	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
40	22	25	V_{SS_2}	S									Digital Ground Voltage		
41	23	26	OSC2	O									Resonator oscillator inverter output		
42	24	27	OSC1	I									External clock input or Resonator oscillator inverter input		
43	25	28	V_{DD_2}	S									Digital Main Supply Voltage		
44	26	29	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI Transmit Data Out	
1	27	30	PE1/RDI	I/O	C_T		X	X			X	X	Port E1	SCI Receive Data In	
2	28	31	PB0	I/O	C_T		X	ei2			X	X	Port B0		
3			PB1	I/O	C_T		X	ei2			X	X	Port B1		
4			PB2	I/O	C_T		X	ei2			X	X	Port B2		
5	29	32	PB3	I/O	C_T		X		ei2		X	X	Port B3		

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD}

are not implemented). See See “I/O PORTS” on page 39. and Section 12.8 I/O PORT PIN CHARACTERISTICS for more details.

3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see Section 1 INTRODUCTION and Section 12.5 CLOCK AND TIMING CHARACTERISTICS for more details.

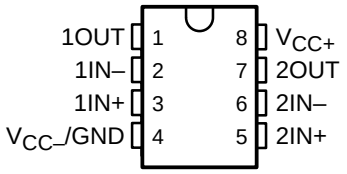
4. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground ($V_{CC–}$)**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ($V_{CC–}$). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

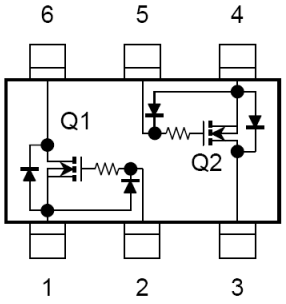
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

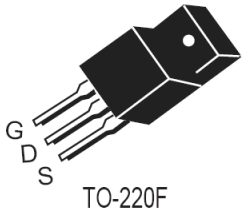
Semiconductors

HN1K05FU N Channel



1. Source 1
2, Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain 1

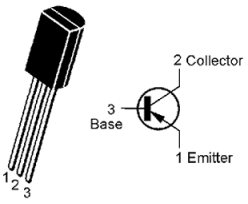
CEF04N6 N Channel



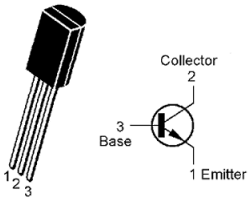
(SCR) MCR100

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

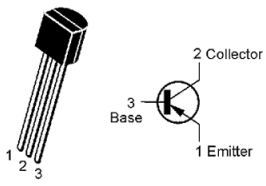
KTA1273Y
KSA916Y



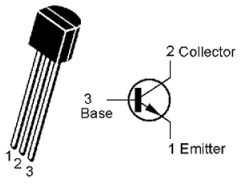
KTC3206



KRC102M
KRC107
KRA102M
KSA708Y



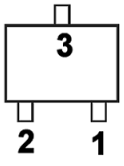
KSC1008Y
KTC3198Y



KSB1151Y

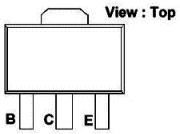
1. Emitter
2. Collector
3. Base

KTC3875S NPN
KTA1504S PNP
KRA107S PNP
KTD1304 NPN
2N3904S NPN
KRC 107S NPN



1) Emitter
2) Base
3) Collector

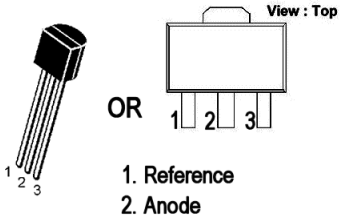
KTA1664



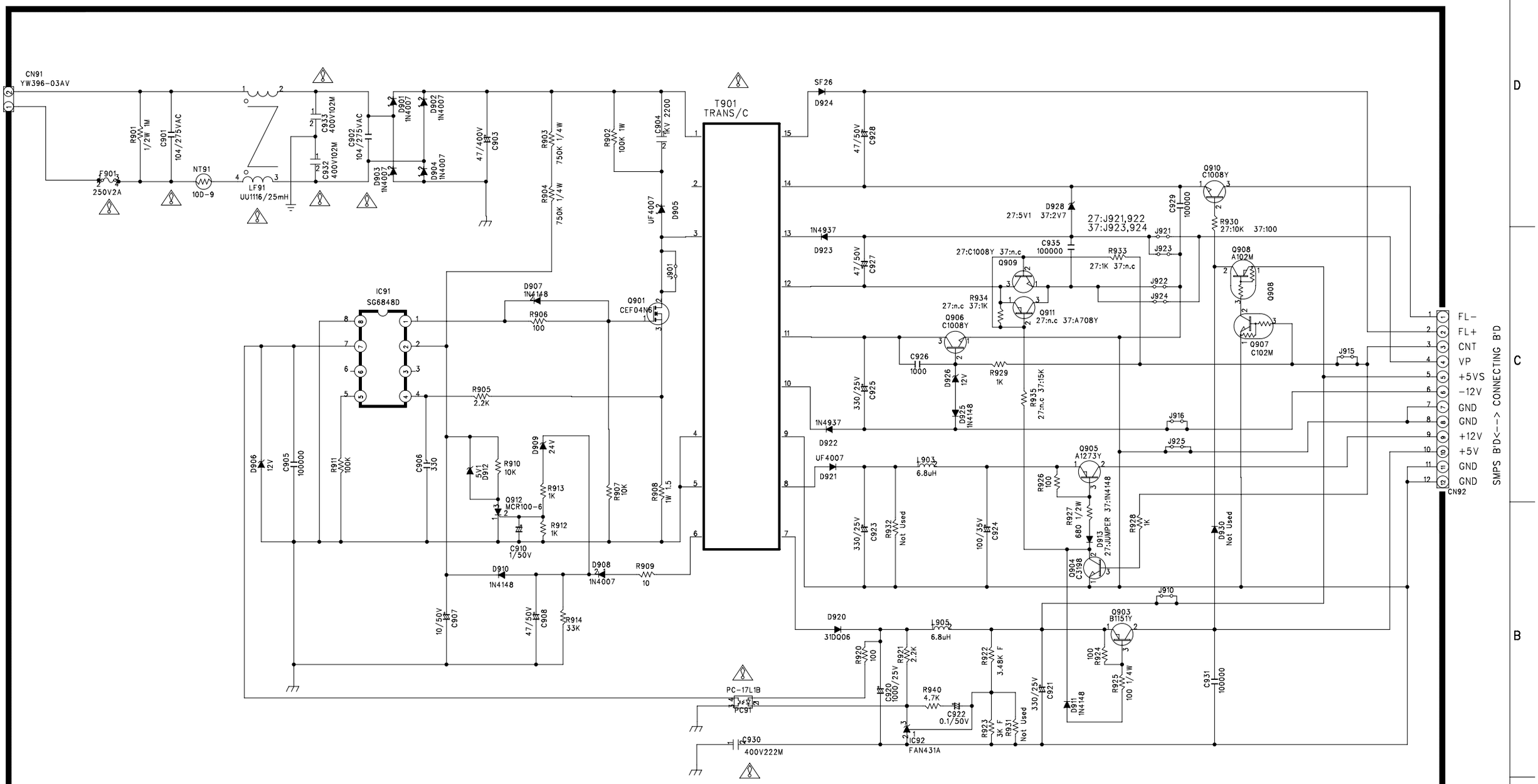
1 Base
2 Collector
3 Emitter

KIA432B

TO-92 SOT-89



1. Reference
2. Anode
3. Cathode



**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS.
USE ONLY MANUFACTUREY'S SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
1pF = 10^{-6} uF

**THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANYTIME
WITH THE IMPROVEMENT OF PERFORMANCE

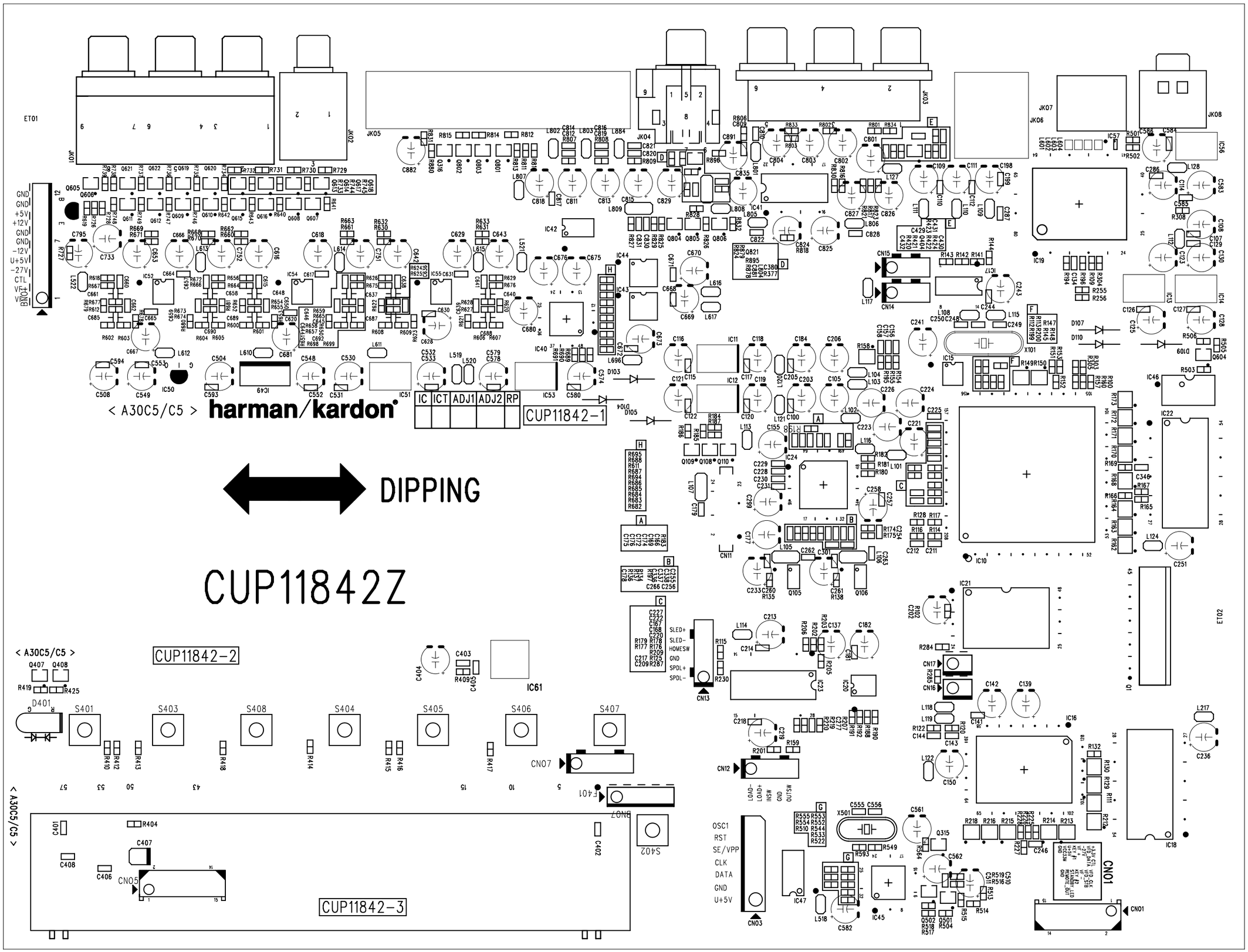
2006.01.17

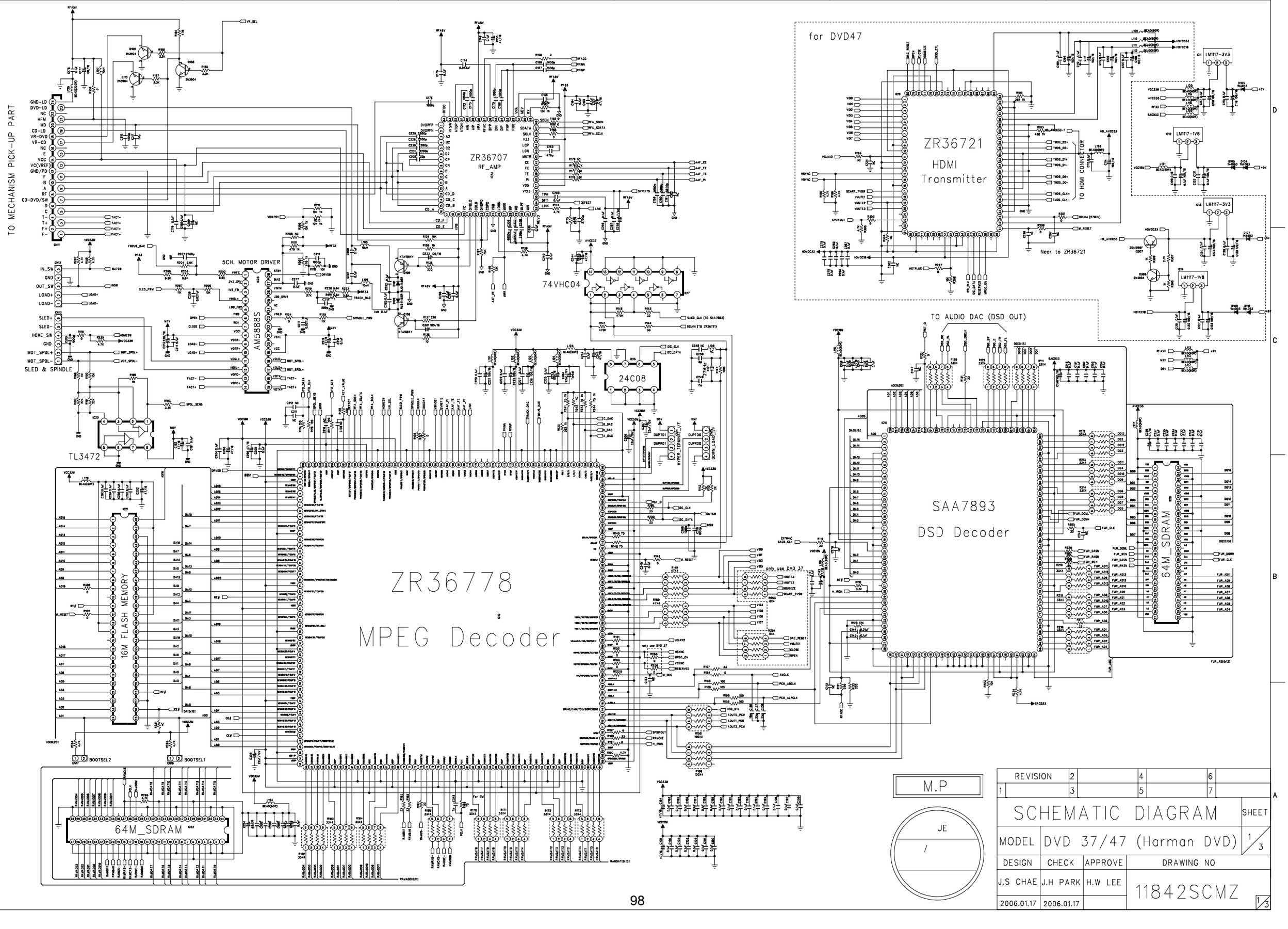
M.P

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM — SHEET

MODEL	DVD 27/37/47		
DESIGN	CHECK	APPROVE	DRAWING NO
S.M.KIM	J.H.PARK		11840SCMZ
06.01.17	06.01.17		(SMPS) 1/1





REVISION	2		4		6		
1	3		5		7		

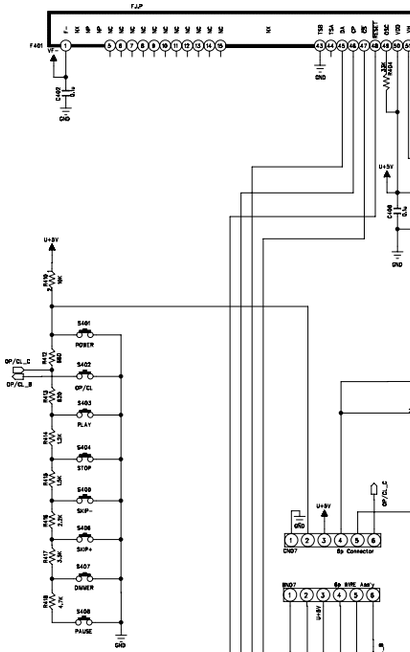
M.P

JE

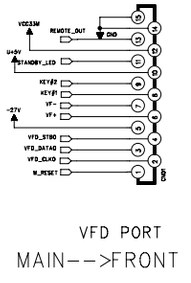
/

SCHEMATIC DIAGRAM SHEET

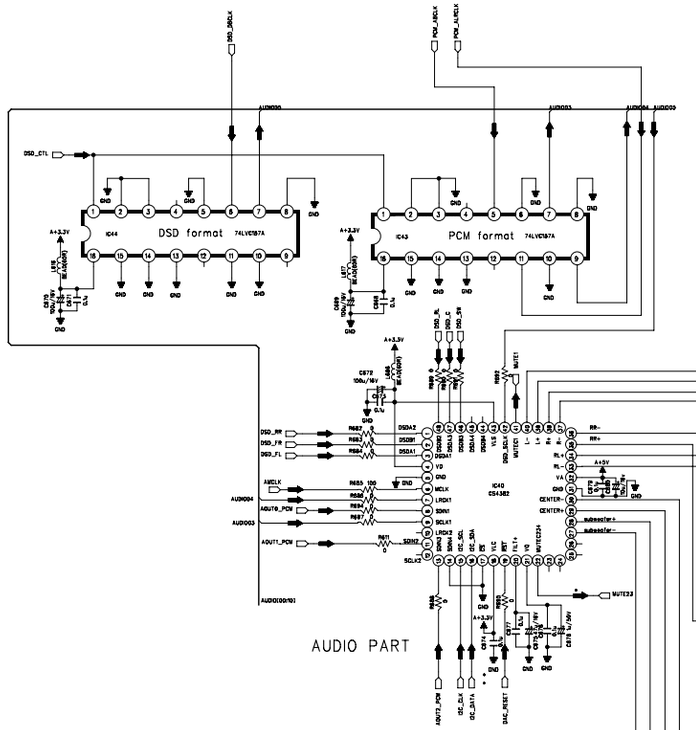
MODEL	DVD 37/47 (Harman DVD)		1/3
DESIGN	CHECK	APPROVE	DRAWING NO
J.S CHAE	J.H PARK	H.W LEE	11842SCMZ
2006.01.17	2006.01.17		1/3



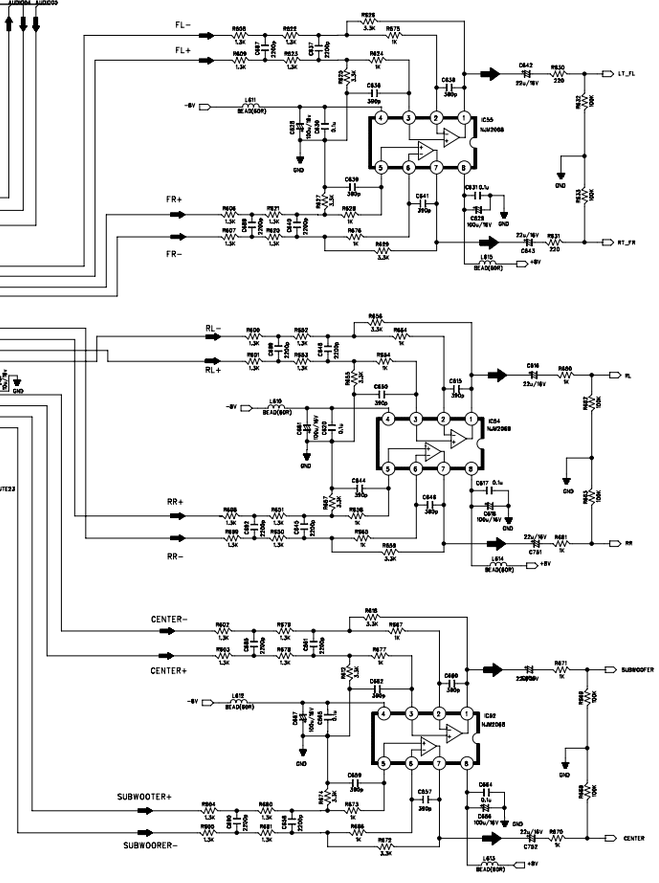
FRONT part

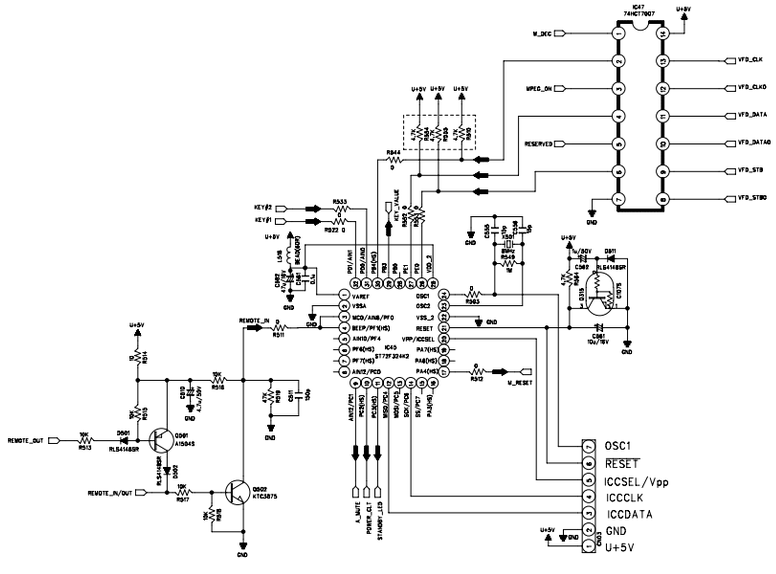


VFD PORT
MAIN-->FRONT

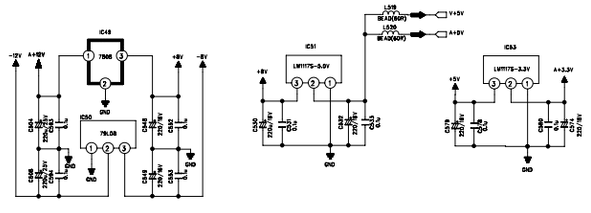


AUDIO PART





MCU PART



POWER PART

REVISION	2		4		6	
1		3		5		7

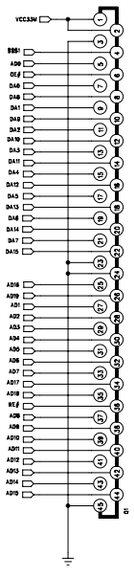
M.P

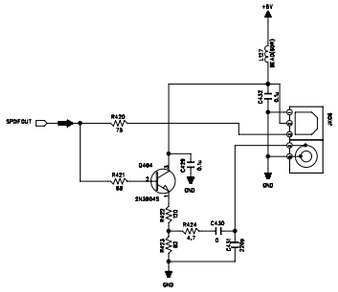
ISSUE

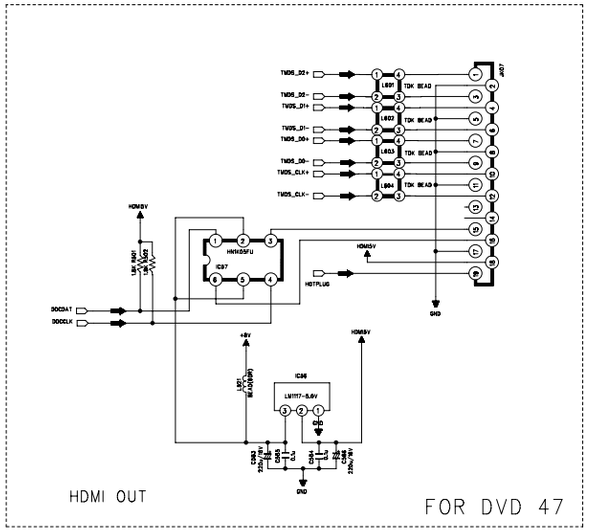
2006.01.17

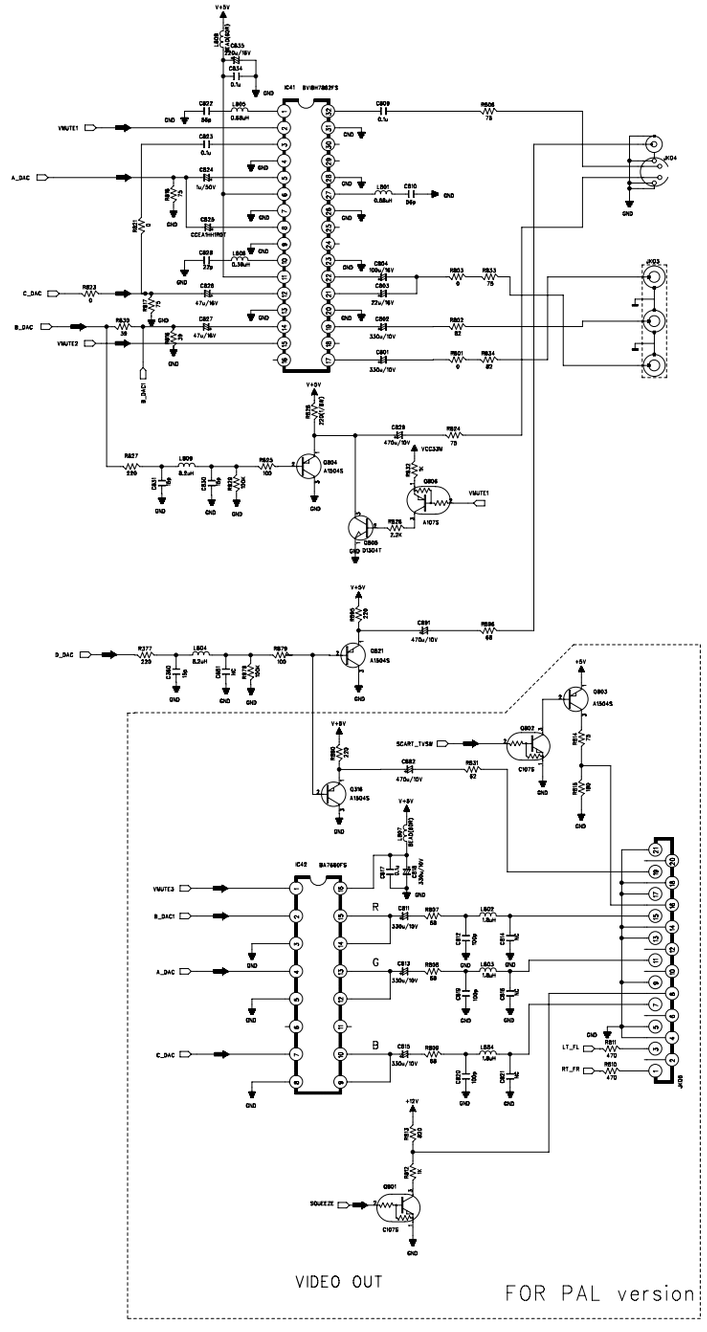
SCHEMATIC DIAGRAM — SHEET 2/3

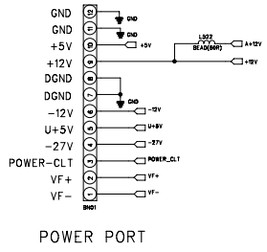
MODEL	DVD 37/47 (Harman DVD)		2/3
DESIGN	CHECK	APPROVE	DRAWING NO
J.S.CHAE	J.H.PARK	H.W.LEE	11842SCMZ
2006.01.17	2006.01.17		2/3

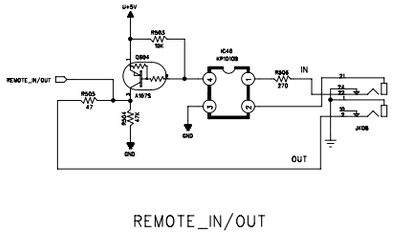


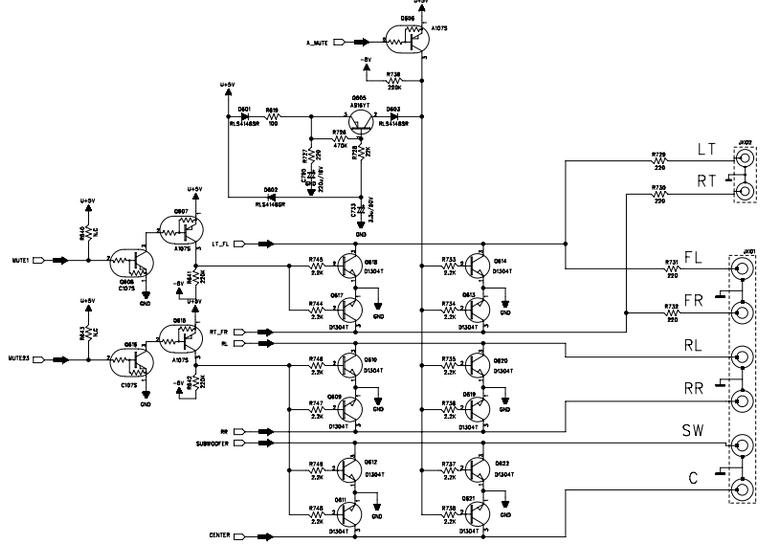












M.P

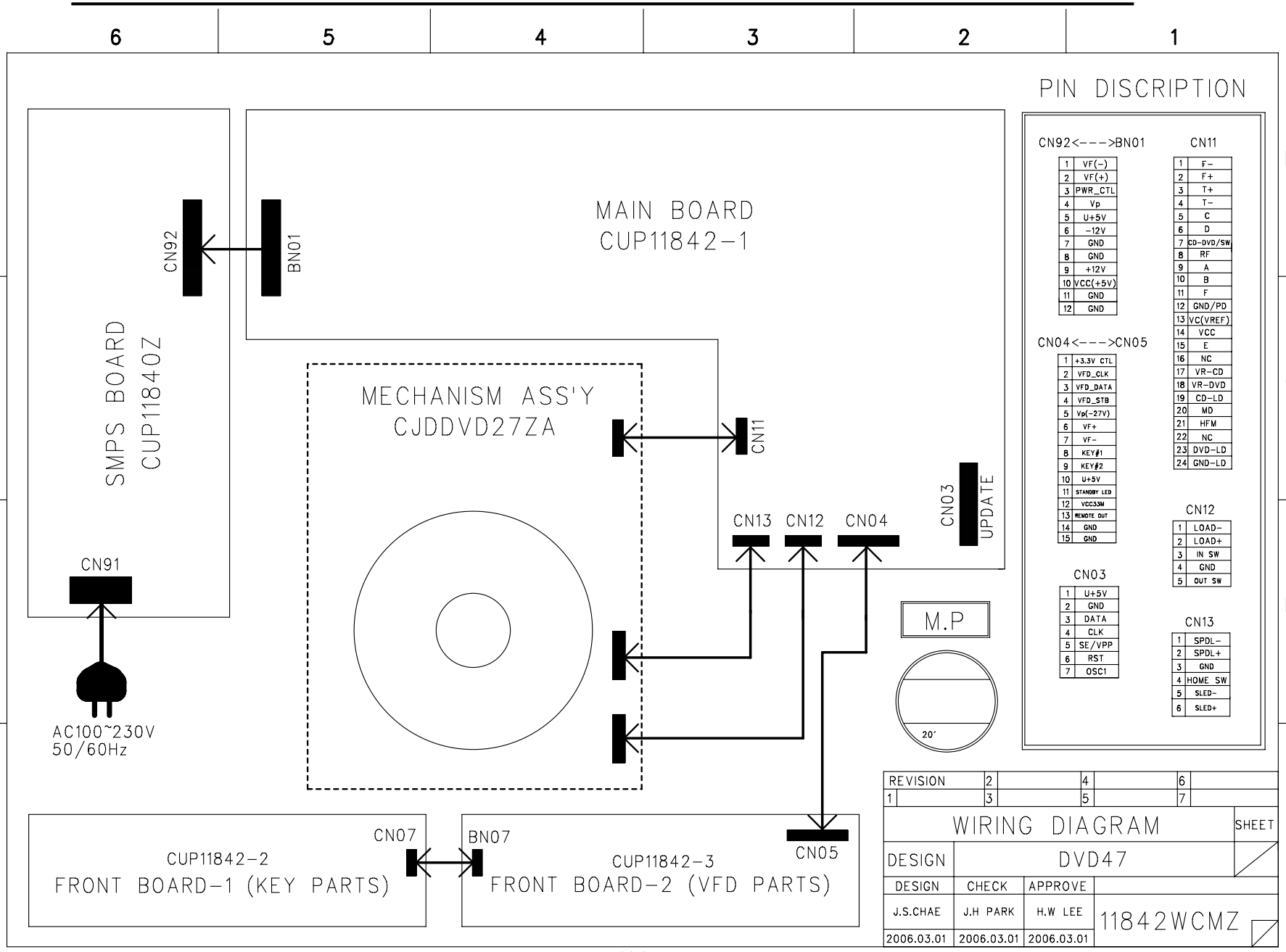
ISSUE

2′

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM — SHEET 3/3

MODEL	DVD 37/47 (Harman DVD)		
DESIGN	CHECK	APPROVE	DRAWING NO
J.S.CHAE	J.H.PARK	H.W.LEE	11842SCMZ 3/3
2006.01.17	2006.01.17		


6
5
4
3
2
1
D
C
B
A
PIN DISCRIPTION
MAIN BOARD
CUP11842-1
SMPS BOARD
CUP11840Z
CN92
BN01
MECHANISM ASS'Y
CJDDVD27ZA
CN11
CN13
CN12
CN04
CN03
UPDATE
CN91
AC100~230V
50/60Hz
M.P
20°
CN92<--->BN01
1 VF(-)
2 VF(+)
3 PWR_CTL
4 Vp
5 U+5V
6 -12V
7 GND
8 GND
9 +12V
10 VCC(+5V)
11 GND
12 GND
CN11
1 F-
2 F+
3 T+
4 T-
5 C
6 D
7 CD-DVD/SW
8 RF
9 A
10 B
11 F
12 GND/PD
13 VC(VREF)
14 VCC
15 E
16 NC
17 VR-CD
18 VR-DVD
19 CD-LD
20 MD
21 HFM
22 NC
23 DVD-LD
24 GND-LD
CN04<--->CN05
1 +3.3V CTL
2 VFD_CLK
3 VFD_DATA
4 VFD_STB
5 Vp(-27V)
6 VF+
7 VF-
8 KEY#1
9 KEY#2
10 U+5V
11 STANDBY LED
12 VCC33M
13 REMOTE OUT
14 GND
15 GND
CN12
1 LOAD-
2 LOAD+
3 IN SW
4 GND
5 OUT SW
CN03
1 U+5V
2 GND
3 DATA
4 CLK
5 SE/VPP
6 RST
7 OSC1
CN13
1 SPDL-
2 SPDL+
3 GND
4 HOME SW
5 SLED-
6 SLED+
CUP11842-2
FRONT BOARD-1 (KEY PARTS)
CN07
BN07
CUP11842-3
FRONT BOARD-2 (VFD PARTS)
CN05
REVISION
WIRING DIAGRAM
SHEET
DESIGN
DVD47
DESIGN
CHECK
APPROVE
J.S.CHAE
J.H PARK
H.W LEE
2006.03.01
2006.03.01
2006.03.01
11842WCMZ